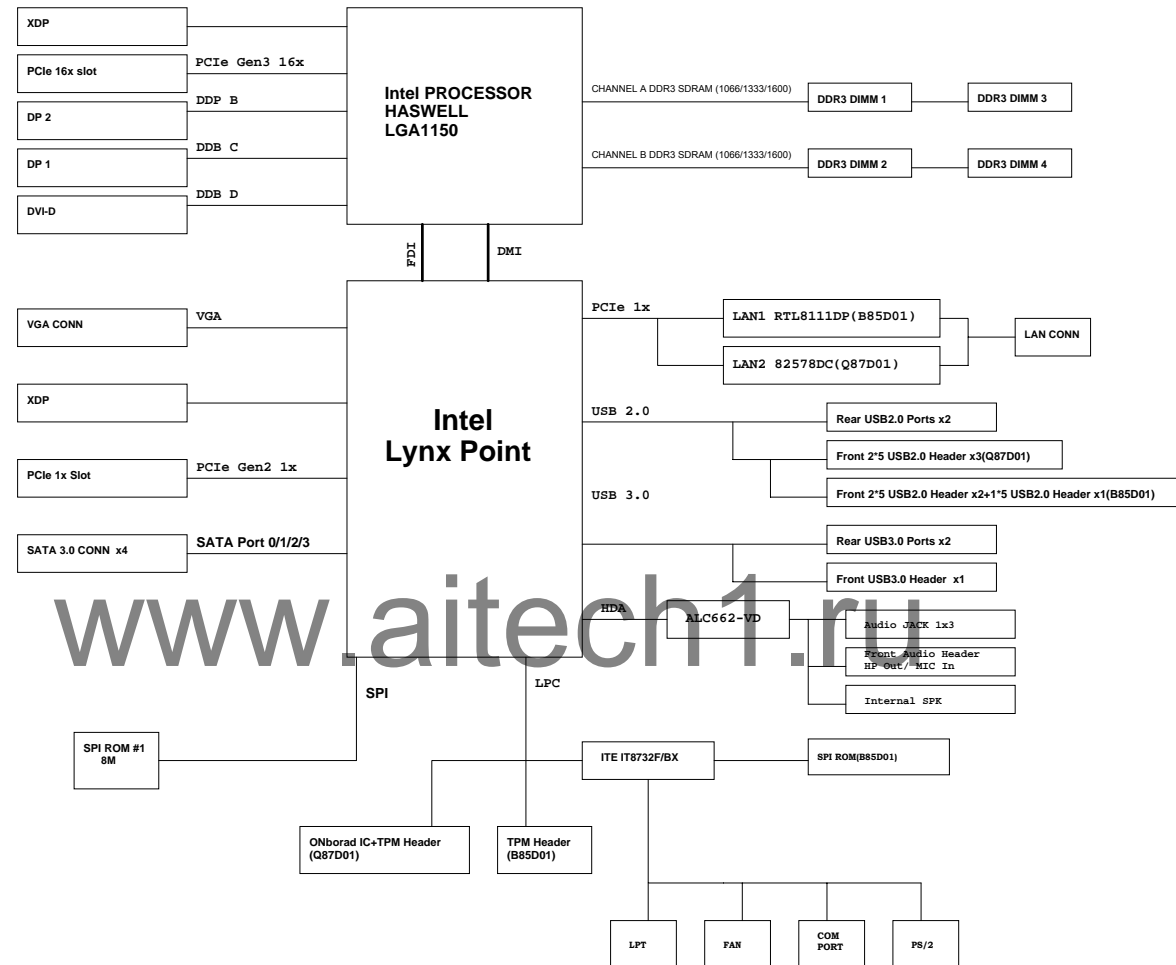


# Spartan

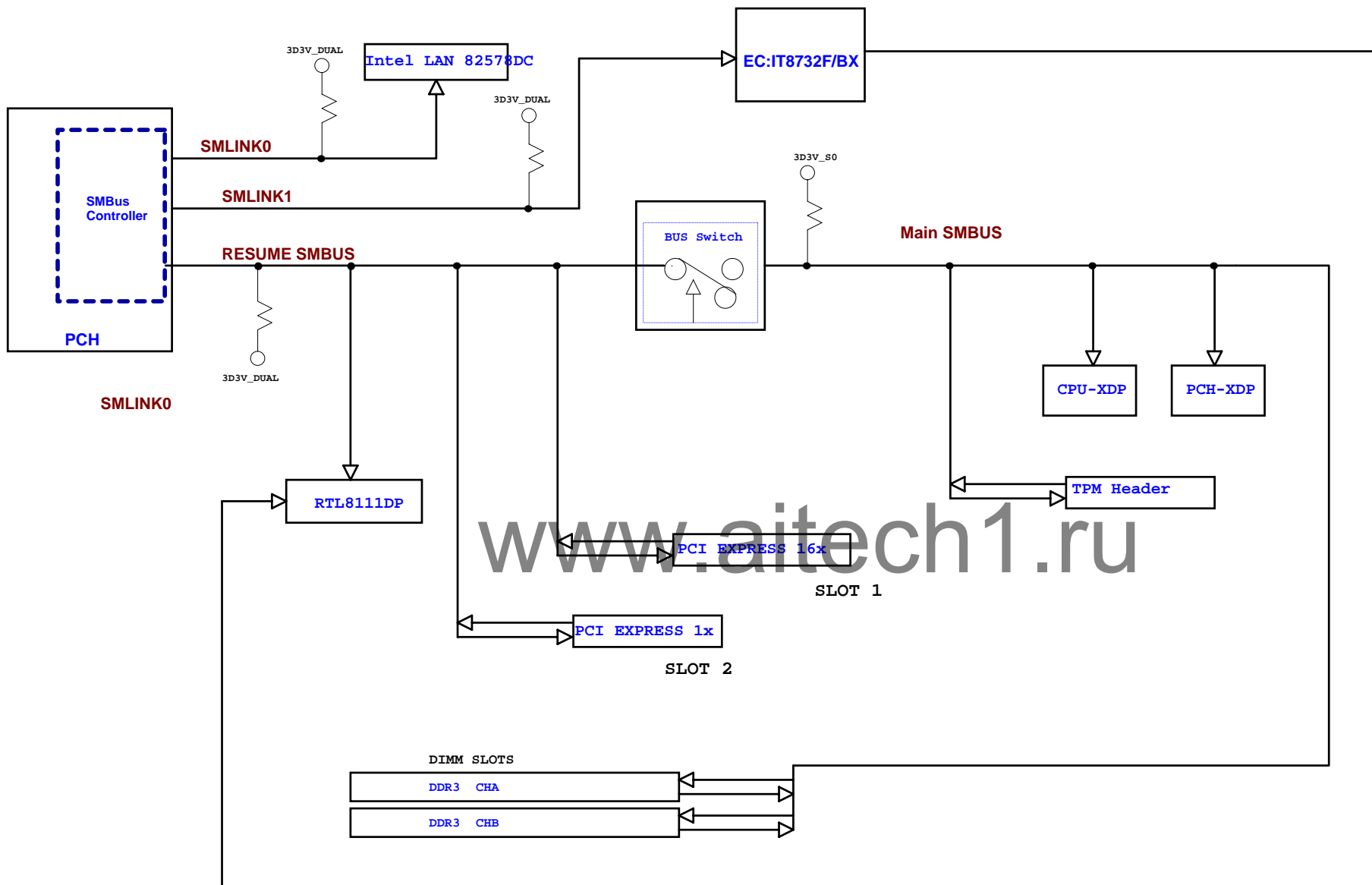
1. Index / Block diagram
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9. GPIO Table
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29. EC-IT8516E/FX
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31. AUDIO\_ALC622VD
32. AUDIO\_CONN/SPK
33. LAN1 RTL8111DP
34. LAN2 82578DC
35. NIC\_USB
36. Slot1: PCIe 16x & 1x
37. Display Port x2
38. DVI&VGA
39. USB3.0 Header
40. USB2.0 Header
41. Rear USB\_3.0 Conn
42. FAN & PS/2
43. TPM/COM
44. ATX CONN
45. Power-1: Linear Power-1
46. Power-2: 1.05V\_PCH/ME
47. Power-3: 5V\_DUAL/3D3V\_DUAL
48. Power-4: Vcore PWM
49. Power-5: Vcore Driver
50. power-6: V\_SM
51. 5V\_SYS&3D3V\_SYS
52. SPI\_Socket\_ROM
53. EMI\_MISC\_PARTS
54. Changelist

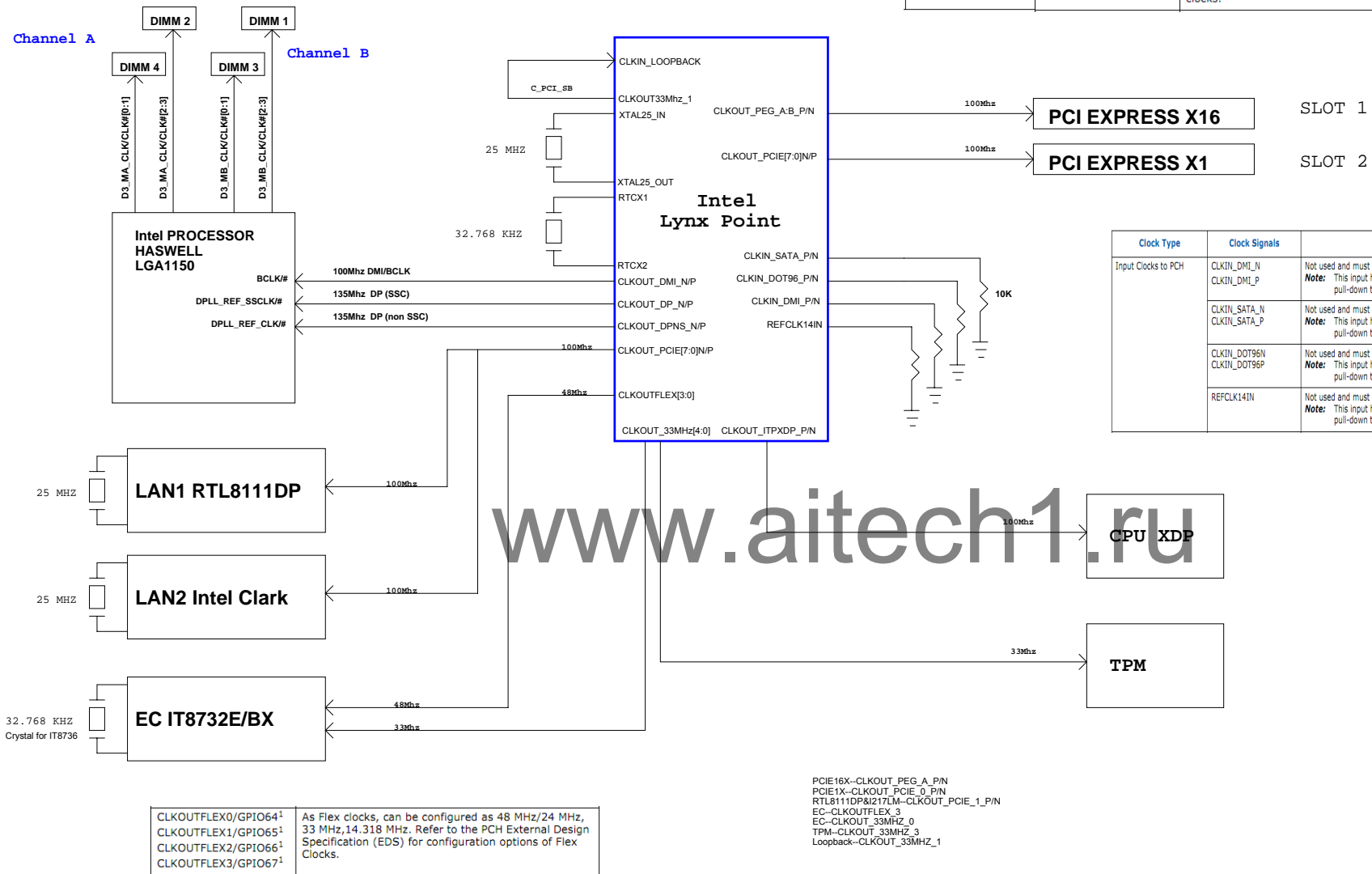
## Reference document

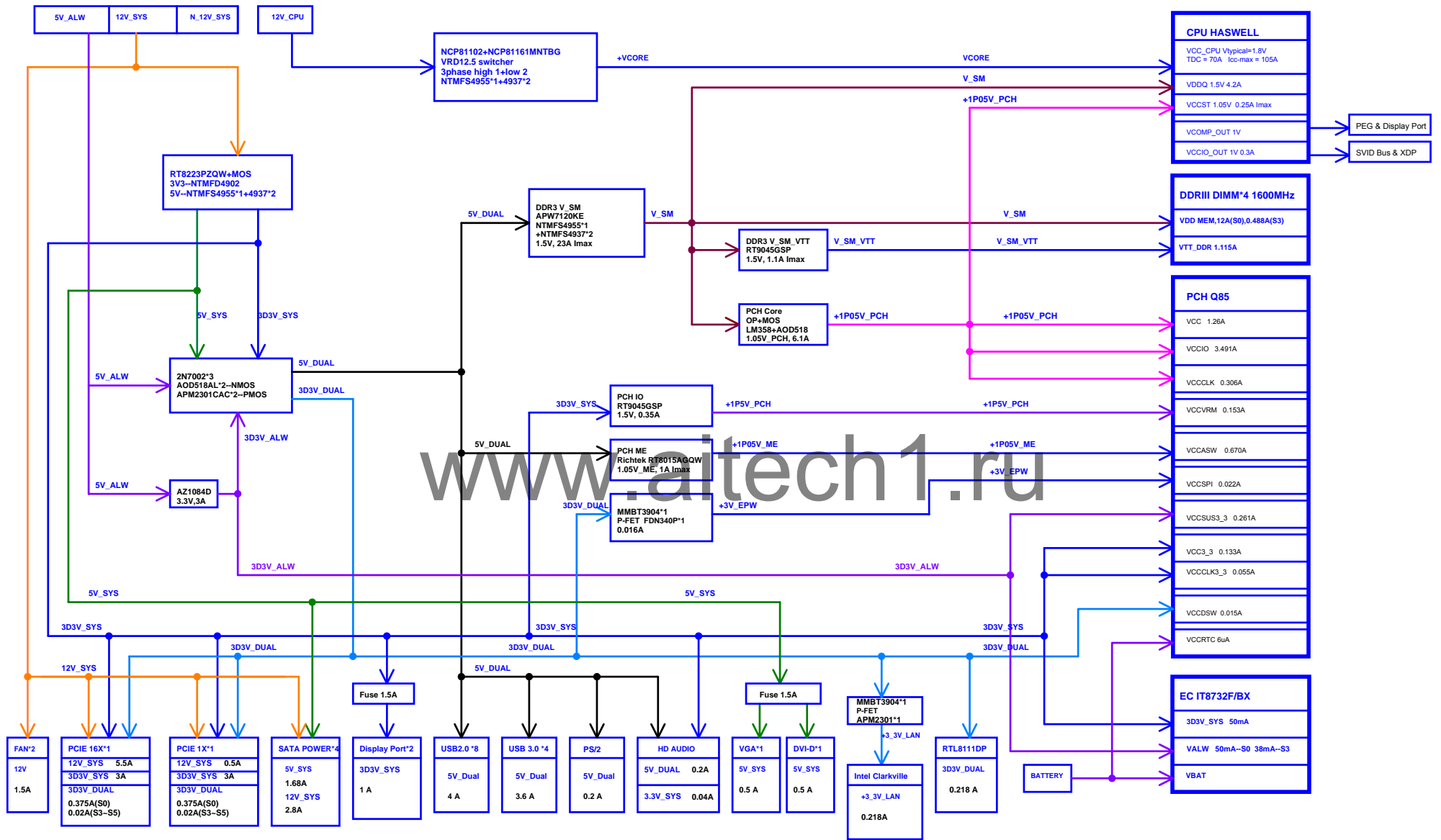
- 1.486711\_486711\_Shark\_Bay\_DT\_PDG\_rev1\_5
- 2.486708\_486708\_LPT\_EDS\_Rev1\_5
- 3.487245\_487245\_HSW\_DT\_EDS\_Vol\_1\_Rev1\_5v1
- 4.453513\_453513\_VR12\_5\_PWM\_Specification\_1\_3
- 5.490765\_490765\_Intel\_2013\_Platform\_SM\_ATLC\_RevOp70
- 6.481476\_Shark\_Bay\_DT\_DenlowWS\_Flathead\_Creek\_CRB\_SCH\_Rev1\_0
- 7.GA-SKB\_051\_INTEL
- 8.SHARKBAY\_VC\_B01\_0517A
- 9.Spartan DTX POR v0.8-20121025
- 10.Acer Mother Board EE Design Request-v6.12-20120731
- 11.Acer DASH support by Realtek v0.2\_12202620



## SMBUS DIAGRAM





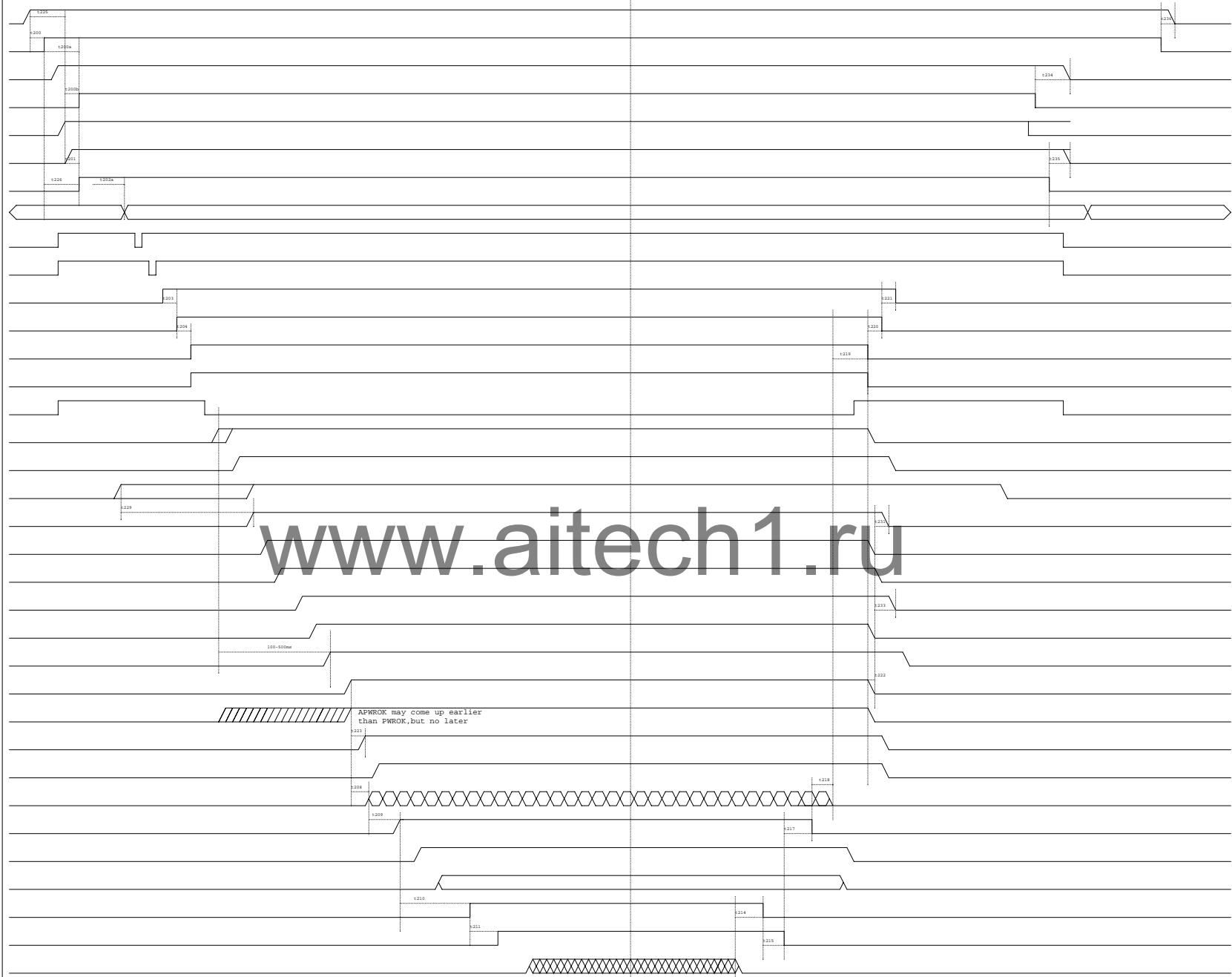


## Power Rail

Power Rail	S0	S3	S4	S5	G3
12V_SYS	O	X	X	X	X
5V_ALW	O	O	O	O	X
N_12V_SYS	O	X	X	X	X
12V_CPU	O	X	X	X	X
VCORE	O	X	X	X	X
3D3V_ALW	O	O	O	O	X
5V_SYS	O	X	X	X	X
3D3V_SYS	O	X	X	X	X
5V_DUAL	O	O	O	O--NO_EUP X--EUP	X
3D3V_DUAL	O	O	O	O--NO_EUP X--EUP	X
V_SM	O	O	X	X	X
V_SM_VTT	O	X	X	X	X
+1P05V_PCH	O	X	X	X	X
+1P05V_ME	O				X
+1P5V_PCH	O	X	X	X	X
+3V_EPW	O				
5V_SYS_DVI	O	X	X	X	X
+3_3V_LAN	O	O	O	O--NO_EUP X--EUP	X
LAN_VDD33	O	O	O	O--NO_EUP X--EUP	X
H_CPU_VCCIO_RIGHT	O	X	X	X	X
VCOMP_OUT_CPU	O	X	X	X	X
+VCCIO2PCH	O	X	X	X	X
VCCST	O	X	X	X	X
DIMMA_DQ_VREF	O	X	X	X	X
DIMMA_CA_VREF	O	X	X	X	X

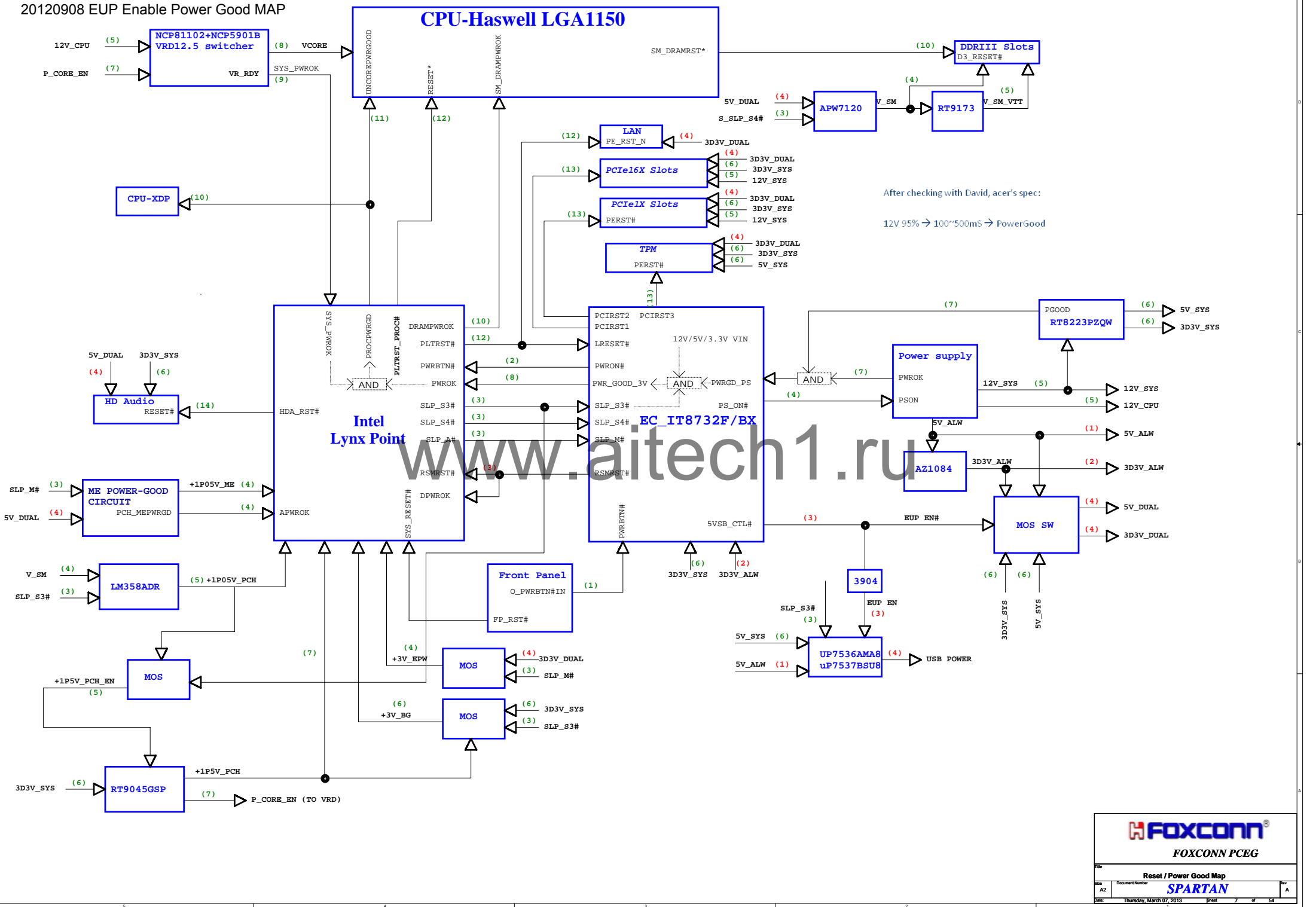
Without Deep S4/S5 sequence

Source	Destination	Signal Name
MB	PCH	VccRTC
MB	PCH	RTCRST#
MB	MB/SIO	5V_ALN 3d3V-ALN
MB	PCH	DPWROK
PCH	SIO	EUP-CTRL
MB	PCH	3d3V-dual
MB	PCH	RSMRST#
PCH	MB	SUSCLK
MB	EC	PWRBTN#
EC	PCH	PWRON#
PCH	MB	SLP_S5#
PCH	MB	SLP_S4#
PCH	MB	SLP_S3#
PCH	MB	SLP_M#
EC	PSU	PS_ON#
PSU	MB	12V/5V/ 3d3V_SYS
VRs	MB/CPU	VDDQ (V_SM)
VRs	PCH	VccASW (+1P05V_ME)
VRs	MB/PCH	PCH VCC (+1P05V_PCH)
VRs	MB/PCH	PCH IO (+1P5V_PCH)
MB	VRD12.5	VR_EN
VRD12.5	CPU	VCC (+VCORE)
VRD12.5	PCH	SYS PWROK (P_VR_READY)
PSU	SIO	ATXPGD
SIO	PCH	PWROK (PWRGD_3V)
MB	PCH	APWROK (PCH_MEPWRGD)
PCH	CPU	DRAMPWROK
CPU	DRAMs	SM_DRAMRST#
PCH	CPU	BCLK, PCIECLKs
PCH	CPU	PROC PWROK (H_PWRGOOD)
CPU	MB	VCCIO_OUT VCOMP_OUT
CPU	VRD12.5	SVIDs
CPU	MB	SUS_STAT#
PCH	CPU	PLTRST#
CPU	PCH	DMI



FOXCONN PCEG

Power On Sequence			
Rev	Document Number	Rev	Rev
A2	SPARTAN	A	A
Date: Thursday, March 07, 2013 Sheet 6 of 54			



## STRAPPING Table

### CPU side

CFG[17:0]	Description	
[2]	PCI Express static x16 lane numbering reversal	1: normal <b>Default</b> 0: lane numbers reversed
[6:5]	PCI Express Bifurcation	00: 1x8, 2x4 PCI Express 01: reserved 10: 2x8 PCI Express 11: 1x16 PCI Express <b>Default</b>

Table 34-6. PCH Digital Display Strapping Signals

Checklist Item	Recommendations	Direction	Comments
DDPC_CTRLDATA	<p>Straps for digital port B, C and D.</p> <p>For DisplayPort* - Should be pulled to 3.3V through a 2.2K W resistor to configure digital port.</p> <p>For DVI/HDMI configuration, the signal should be routed through the level shifter to the display connector. The signal is pulled to 3V before the level shifter and 5V before the display connector through a 2.2K W resistor. This signal should always be routed longer than DDPC_CTRLCLK by an inch.</p> <p>For DVI/HDMI configuration with the Cost Reduced level shifter, the signal should be routed through the pass gate sourced from 3.3V voltage. The signal is pulled to 3V before the pass gate and 5V before the display connector through a 2.2K W resistor and a Schottky diode. This signal should always be routed longer than DDPC_CTRLCLK by an inch. Also ensure schottky diode is not shared with DDPC_CTRLCLK.</p>	BI	

Table 36-18. Strapping Signals (Sheet 1 of 2)

Name	Type	Recommendations	Reason/Impact
SPKR	I	<b>Default Mode:</b> Internal weak Pull-down.  <b>No Reboot Mode with TCO Disabled:</b> Connect to Vcc3_3 with 8.2k-10k Ohm weak pull-up resistor.	
INIT3_3V#	I	Do not pull low.	
GPIO55	I/O	<b>Default Mode:</b> Internal pull-up.  <b>Top Block Swap Mode:</b> Connect to ground with 4.7k Ohm weak pull-down resistor.	
SATA1GP/ GPIO19, GPIO51	I/O	<b>Default (SPI)</b> Left both SATA1GP/GPIO19 and GPIO51 floating. No pull up required.  <b>Boot from PCI</b> Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor. Leave GPIO51 Floating.  <b>Boot from LPC</b> Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.	If LPC is selected BIOS may still be placed on LPC, but all platforms with PCH require SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot.  Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN.
GPIO53	I/O	Do not pull low. Connect to ground with 1k Ohm pull-down resistor.	ESI strap for server platform ONLY
HDA_SDO	I/O	<b>Default:</b> Do not pull high.  <b>Disable ME in Manufacturing Mode</b> Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.	Flash descriptor Override
SPI_MOSI	I/O	Internal weak pull down. Do not pull high.	DME RX Termination Voltage
SAAT3GP/ GPIO37	I/O	<b>Enable TLS:</b> Pull up with 1k Ohm to VccSus3.3. <b>Default (Disable TLS):</b> Leave NC. Internal pull down.	TLS confidentiality
GPIO8	I/O	Internal weak pull up. Do not pull low.	

Table 36-18. Strapping Signals (Sheet 2 of 2)

Name	Type	Recommendations	Reason/Impact
GPIO62/ SUSCLK	I/O	Internal weak pull up. Do not pull low.	On die PLL voltage regulator
GPIO36	I/O	Internal weak pull down. Do not pull high.	
DDPB_CTRL_DATA DDPC_CTRL_DATA DDPD_CTRL_DATA		<p>Straps for digital ports B, C and D.</p> <p>For DisplayPort* - Should be pulled to 3.3V through a 2.2k ohms resistor to configure digital port.</p> <p>For DVI/HDMI configuration, the signal should be routed through the level shifter to the display connector. The signal is pulled to 3V before the level shifter and 5V before the display connector through a 2.2k ohms resistor. This signal should always be routed longer than SDVO/DDPC_CTRLCLK by an inch.</p> <p>For DVI/HDMI configuration with the Cost Reduced level shifter, the signal should be routed through the pass gate sourced from 3.3V voltage to the display connector. The signal is pulled to 3V before the pass gate and 5V before the display connector through a 2.2k ohms resistor. This signal should always be routed longer than SDVO/DDPC_CTRLCLK by an inch.</p>	

#### Strapping Options Flash

Option	Minimum Voltage	Setting
1	0	Flash (pins Resistor to GND)
2	0	Flash (pins Resistor to VCC)
3	0	Flash (pins Resistor to GND) <b>Default</b>





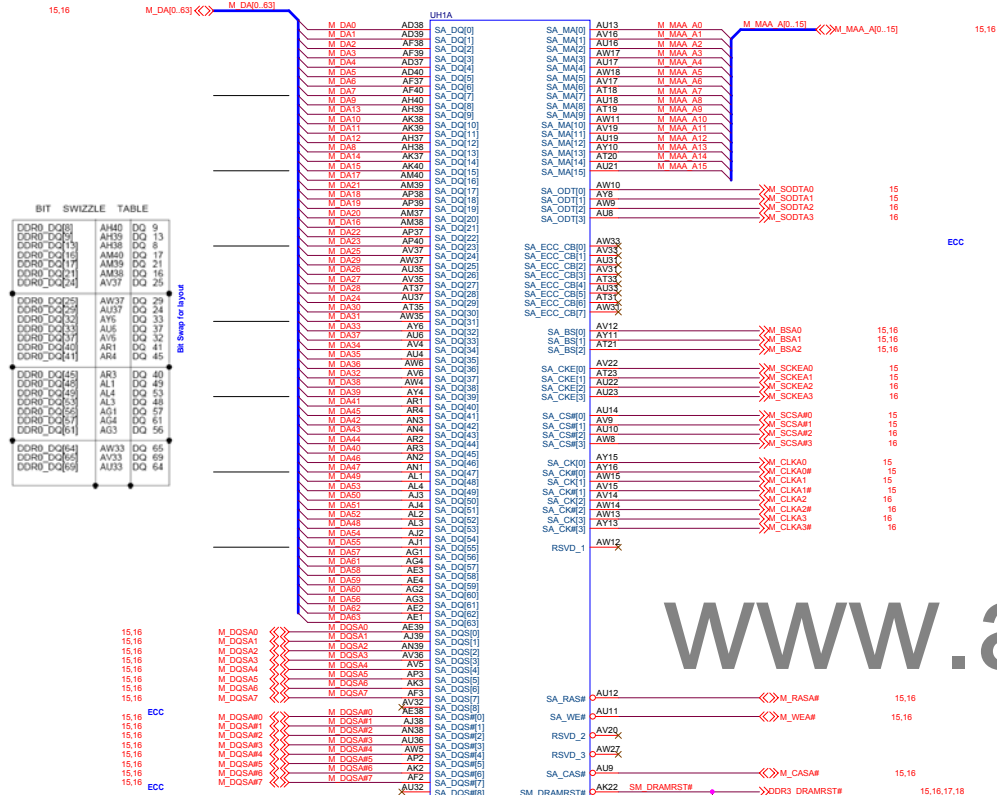
# PCH GPIO Table

1	GPIO0	G38	I/O	A_FP_AUDIO_PRESENCE#	8.2K TO 3D3V_SYS
2	GPIO1	AT31	I/O	PCH_GPIO1	10K TO 3D3V_SYS Board ID
3	GPIO[5:2]	AT27/AV28/AV29/AR30	I/O	PCH_GPIO[5:2]	8.2K TO 3D3V_SYS
4	GPIO[7:6]	AV34/AM28	I/O	PCH_GPIO[7:6]	10K TO 3D3V_SYS
5	GPIO8	AC40	I/O	IGC_EN_N	XDP
6	GPIO9	AC41	I/O	U_USB_OC_R_#5	8.2K to 3D3V_DUAL Connect to XDP
7	GPIO10	AF40	I/O	U_USB_OC_R_#6	8.2K to 3D3V_DUAL Connect to XDP
8	GPIO11	AG31	I/O	SMBALERT#	10K TO 3D3V_ALW Connect to RTL8111DP
9	GPIO12	AL40	I/O	LAN_DISABLE#	10K(EMPTY) to +3_3V_LAN Connect to LAN disable
10	GPIO13	AN22	I/O	PCH_GPIO13	10K TO 3D3V_ALW
11	GPIO14	AG40	I/O	U_USB_OC_R_#7	8.2K to 3D3V_DUAL Connect to XDP
12	GPIO15	AC32	I/O	PCH_GPIO15	10K TO 3D3V_ALW
13	GPIO16	M39	I/O	SATA4GP	10K TO 3D3V_SYS PCIE SATA Strap
14	GPIO17	AP28	I/O	PCH_GPIO17	10K TO 3D3V_SYS Board ID
15	GPIO18	P39	I/O	PCH_GPIO18	10K TO GND XDP
16	GPIO19	J40	I/O	SATA1GP	10K TO 3D3V_SYS XDP
17	GPIO20	P37	I/O	PCH_SMI_N	10K TO 3D3V_SYS XDP
18	GPIO21	M37	I/O	SATA0GP	10K TO 3D3V_SYS XDP
19	GPIO22	L38	I/O	S_PCH_CONFIG_JUMPER	1K TO 3D3V_SYS
20	GPIO23	AK26	I/O	PCH_L_DRQ_1#	EMPTY
21	GPIO24	AE34	I/O	H_SKTOCC#	10K TO 3D3V_ALW
22	GPIO25	AA39	I/O	PCH_GPIO25	10K TO 3D3V_ALW
23	GPIO26	W35	I/O	PCH_GPIO26	10K TO 3D3V_ALW
24	GPIO27	AU34	I/O	LAN_WAKE_N	TO LAN
25	GPIO28	V41	I/O	A_FP_PRES#	10K TO 3D3V_ALW
26	GPIO29	AL39	I/O	PCH_GPIO29	EMPTY
27	GPIO30	AG41	I/O	S_SUSWARN#	TO S_SUSACK#
28	GPIO31	AM36	I/O	S_PSWD_SLR	10K TO 3D3V_ALW
29	GPIO32	N32	I/O	PCH_GPIO32	EMPTY
30	GPIO33	AV26	I/O	PCH_GPIO33	EMPTY
31	GPIO34	N34	I/O	PCH_GPIO34	10K TO 3D3V_SYS
32	GPIO35	M40	I/O	2X4_POWER_DETECT	XDP
33	GPIO[37:36]	N41/H40	I/O	PCH_GP[37:36]	1K TO 3D3V_SYS
34	GPIO38	H41	I/O	PCH_GPIO38	S_MFG_MODE_OR
35	GPIO39	R31	I/O	PCH_GPIO39	10K TO 3D3V_SYS

36	GPIO[43:40]	AF39/AD40/AD39/AF37	I/O	U_USB_OC_R_#[4:1]	TO USB XDP
37	GPIO44	AA36	I/O	S_INTRUD_CBL_DET#	10K TO 3D3V_ALW
38	GPIO45	W32	I/O	PCH_GPIO45	10K TO 3D3V_ALW
39	GPIO46	AA40	I/O	PCH_GPIO46	10K TO 3D3V_ALW
40	GPIO47		I/O		
41	GPIO48	L40	I/O	PCH_GPIO48	10K TO 3D3V_SYS
42	GPIO49	N40	I/O	PCH_GPIO49	10K TO 3D3V_SYS
43	GPIO50	AH26	I/O	PCH_GPIO50	8.2K TO 3D3V_SYS
44	GPIO51	AU31	I/O	PCH_GPIO51	EMPTY
45	GPIO52	AJ26	I/O	PCH_GPIO52	8.2K TO 3D3V_SYS
46	GPIO53	AV31	I/O	PCH_GPIO53	EMPTY
47	GPIO54	AW33	I/O	PCH_GPIO54	8.2K TO 3D3V_SYS
48	GPIO55	R30	I/O	PCH_GPIO55	EMPTY
49	GPIO56		I/O		
50	GPIO57	AC36	I/O	PCH_GPIO57	10K TO 3D3V_ALW
51	GPIO58	AK36	I/O	SML1CLK	2.2K TO 3D3V_ALW
52	GPIO59	AE40	I/O	U_USB_OC_R_#0	TO USB
53	GPIO60	AG35	I/O	SMI0LALERT#	10K TO 3D3V_ALW
54	GPIO61	AD37	I/O	SUS_STAT#_PCH	LPCPD# TO EC/XDP
55	GPIO62	W36	I/O	SUSCLK_PCH	EMPTY
56	GPIO63	AA35	I/O	S_SLP_S5#	EMPTY
57	GPIO64	AV8	I/O	CLKOUTFLEX0_14M	EMPTY
58	GPIO65	AT9	I/O	CLKOUTFLEX2_14M	EMPTY
59	GPIO66	AV9	I/O	CLKOUTFLEX2	EMPTY
60	GPIO67	AU8	I/O	CLKOUTFLEX3	EMPTY
61	GPIO[69:68]	AV35/AT30	I/O	PCH_GPIO[69:68]	10K TO 3D3V_SYS
62	GPIO[71:70]	AT34/AK28	I/O	PCH_GPIO[71:70]	10K TO 3D3V_SYS
63	GPIO72	AJ40	I/O	PCH_GPIO72	1K TO 3D3V_ALW
64	GPIO73	W34	I/O	PCH_GPIO73	10K TO GND
65	GPIO74	AJ39	I/O	TMIN_SHIFT	10K TO 3D3V_ALW
66	GPIO75	AK33	I/O	SML1DATA	2.2K TO 3D3V_ALW

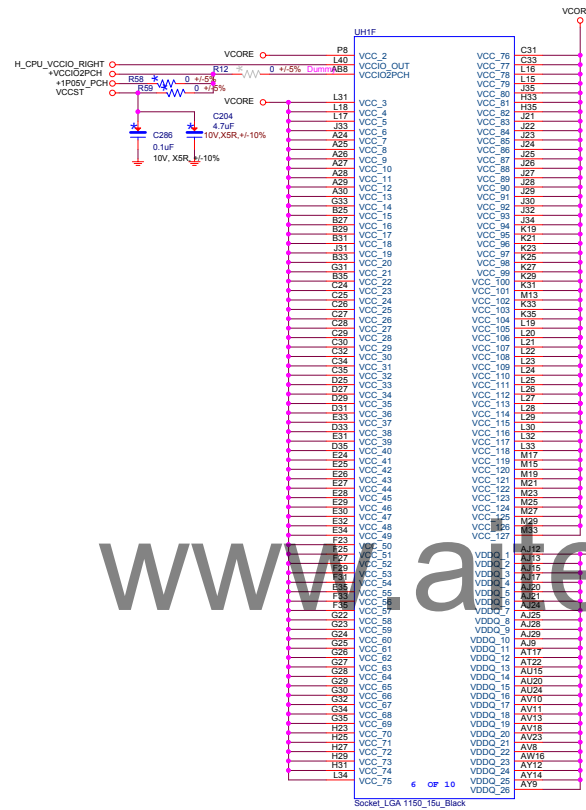
The ECC UDIMM details are ONLY for Denlow-WS processor designs  
Desktop PCH platforms support non-ECC UDIMMs only  
Server PCH platforms support ECC UDIMMs only

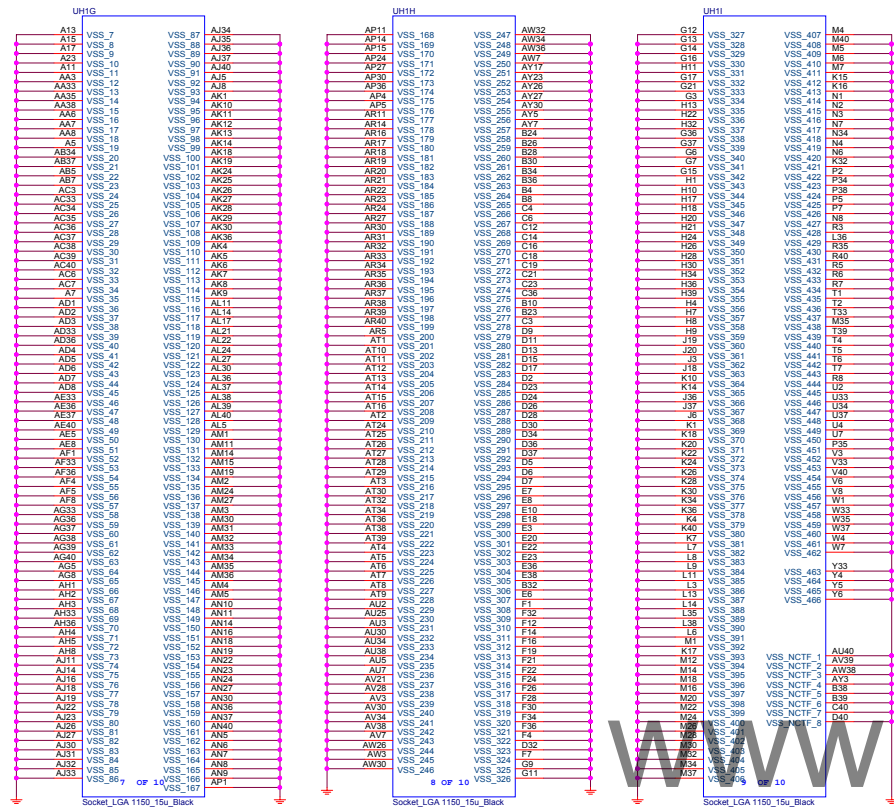
## DDR3 CH-A











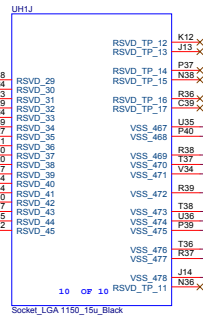
20121109 R1582 change from 2.67K to 2.8K for CPU PWROK level

21.23.29

PWRGD\_3V

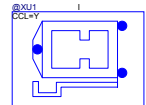
+R270  
6.04K  
+1-1%

+R1582  
2.8K  
+1-1%  
(040224)



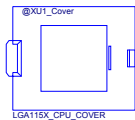
www.aitech1.ru

CPU\_Loading Module (DIP)



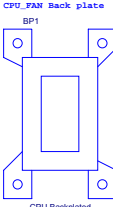
20120027 Cover 1xCPU Socket是配合使用, 需带一个894 PIN

CPU\_Plastic Cover (DIP)

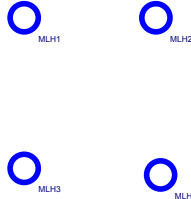


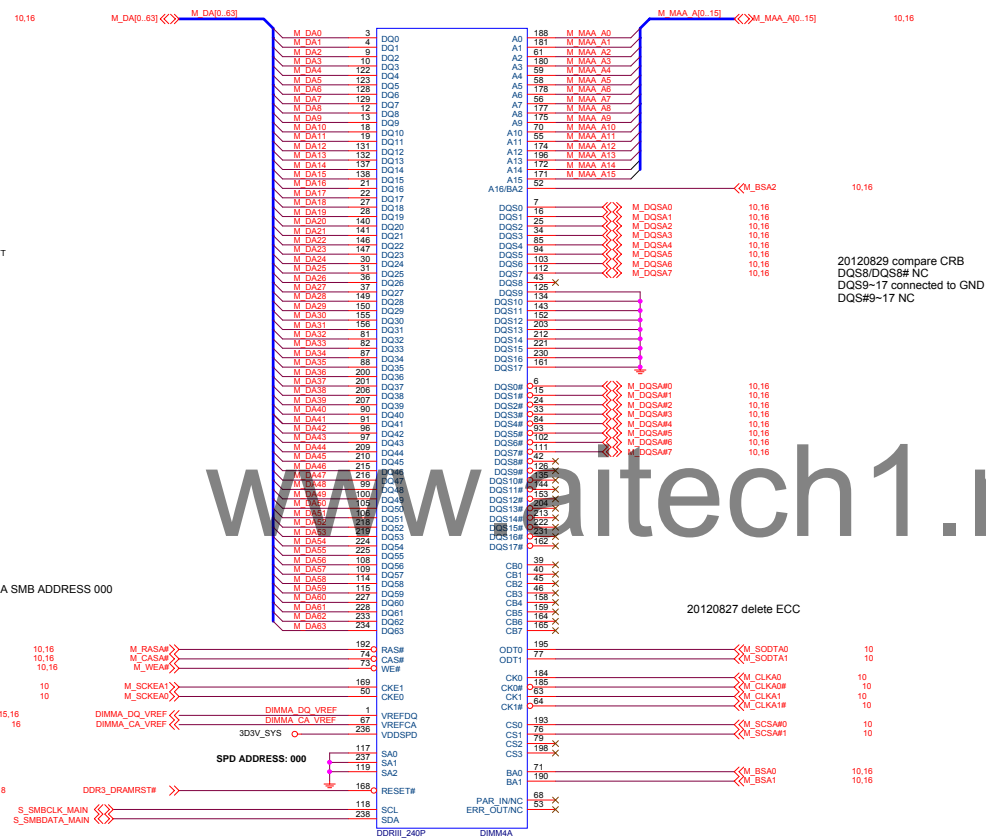
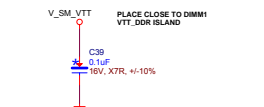
CPU\_FAN Back plate (DIP)

Non-PTH Hole



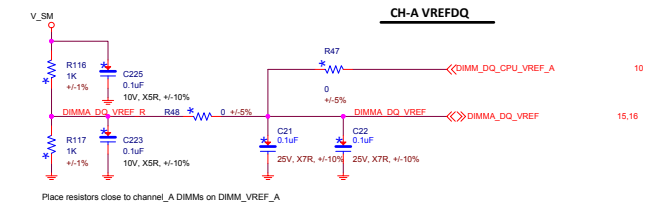
mylar PAD for CPU\_FAN back plate





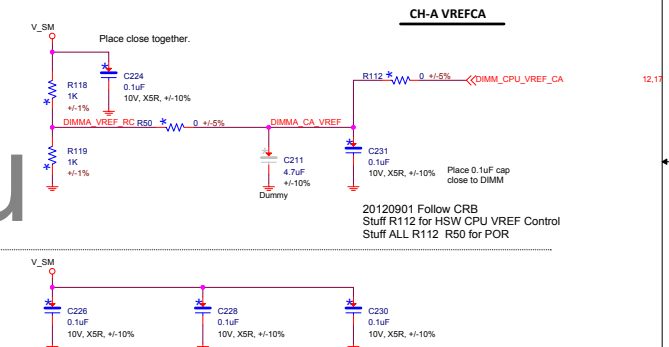
20120901 Follow CRB C21&amp;C22 Change from 0402 to 0603

For future processor compatibility, the total on-board capacitance for VREFDQ per channel should be less than or equal to 0.3 Farads nominal



Place resistors close to channel\_A DIMMs on DIMM\_VREF\_A

20120829 compare CRB  
DQS8/DQS8# NC  
DQS9~17 connected to GND  
DQS#9~17 NC

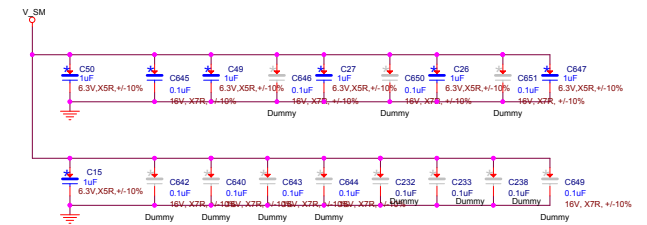
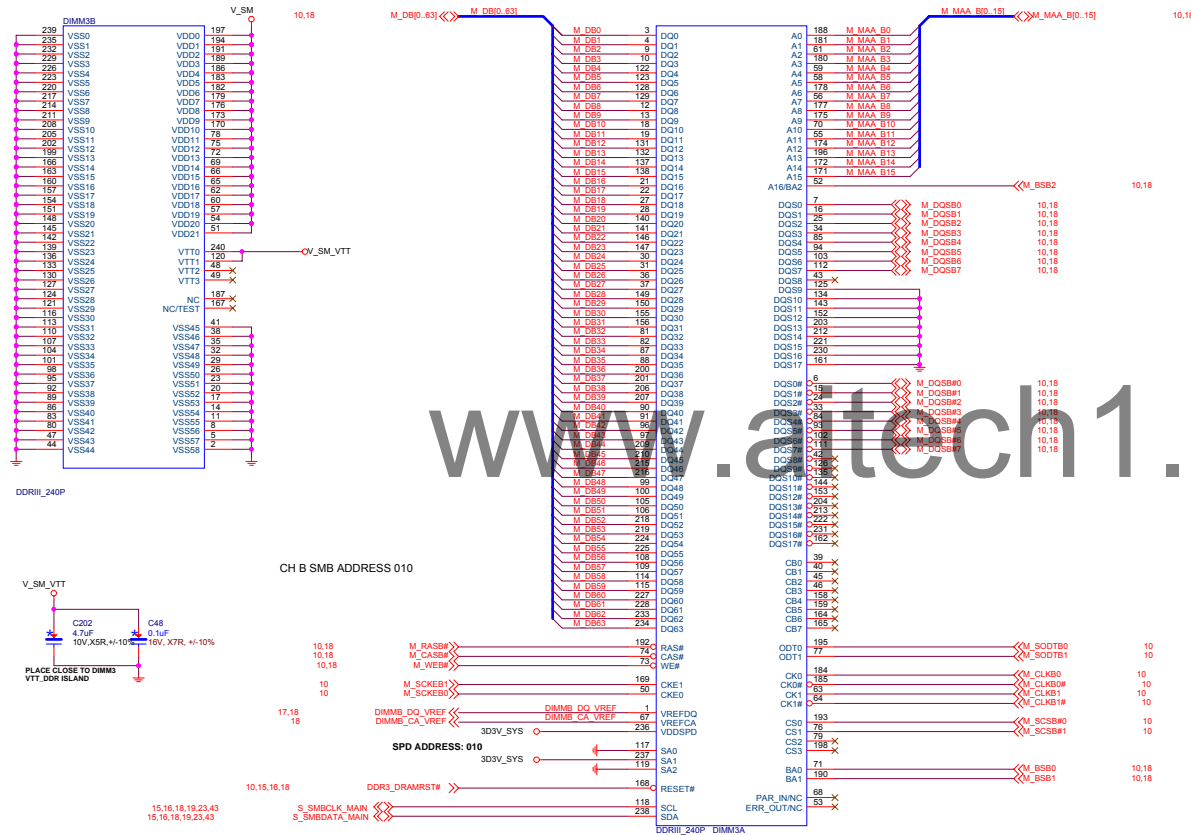


20120901 Follow CRB  
Stuff R112 for HSW CPU VREF Control  
Stuff ALL R112 R50 for POR



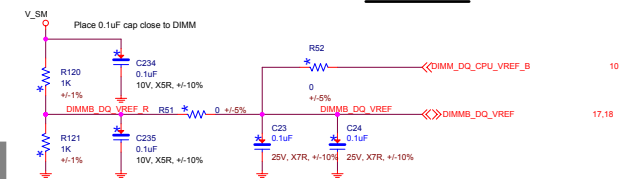






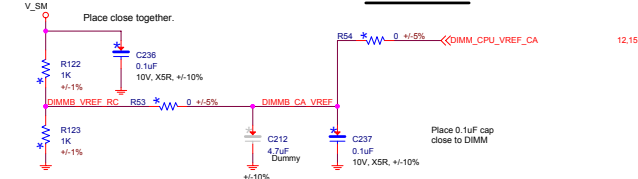
20120901 Follow CRB C23&C24 Change from 0402 to 0603

#### CH-B VREFDQ



20120901 Follow CRB Voltage Divider Option--Stuff R51 VREF Control from CPU--Stuff R52 Need double check R51&R52 exist in which condition

#### CH-B VREFCA

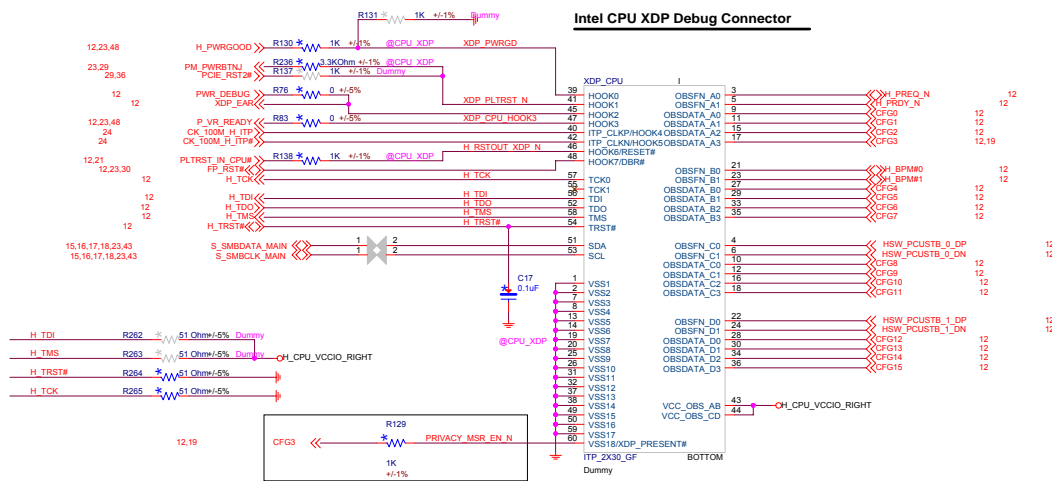


20120901 Follow CRB Stuff R54 for HSW CPU VREF Control Stuff ALL R54 R53 for POR



File		
DDR3 Conn: CHB_1 (DIMM2)		
Rev	Document Number	Rev
A2	SPARTAN	A
Date: Thursday, March 07, 2013 Sheet 17 of 54		





#### Intel PCH XDP Debug Connector

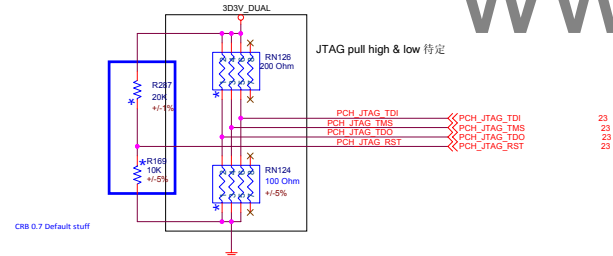


Table 3-1. Processor XDP Connector Pinout

Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	GND	GND	NA		2	GND	GND	NA	
3	OBSFN_A0	PREQ#	I/O	processor	4	OBSFN_C0	CFG[17]#	I	Processor
5	OBSFN_A1	PRDY#	I/O	processor	6	OBSFN_C1	CFG[16]#	I	Processor
7	GND	GND	NA		8	GND	GND	NA	
9	OBSDATA_A0	CFG[0]#	I/O	Processor	10	OBSDATA_C0	CFG[8]#	I/O	Processor
11	OBSDATA_A1	CFG[1]#	I/O	Processor	12	OBSDATA_C1	CFG[9]#	I/O	Processor
13	GND	GND	NA		14	GND	GND	NA	
15	OBSDATA_A2	CFG[2]#	I/O	Processor	16	OBSDATA_C2	CFG[10]#	I/O	Processor
17	OBSDATA_A3	CFG[3]#	I/O	Processor	18	OBSDATA_C3	CFG[11]#	I/O	Processor
19	GND	GND	NA		20	GND	GND	NA	
21	OBSFN_B0	BPM#[0]#	I/O	processor	22	OBSFN_D0	CFG[19]#	I/O	Processor
23	OBSFN_B1	BPM#[1]#	I/O	processor	24	OBSFN_D1	CFG[18]#	I/O	Processor
25	GND	GND	NA		26	GND	GND	NA	
27	OBSDATA_B0	CFG[4]#	I/O	Processor	28	OBSDATA_D0	CFG[12]#	I	Processor
29	OBSDATA_B1	CFG[5]#	I/O	Processor	30	OBSDATA_D1	CFG[13]#	I	Processor
31	GND	GND	NA		32	GND	GND	NA	
33	OBSDATA_B2	CFG[6]#	I/O	Processor	34	OBSDATA_D2	CFG[14]#	I/O	Processor
35	OBSDATA_B3	CFG[7]#	I/O	Processor	36	OBSDATA_D3	CFG[15]#	I/O	Processor
37	GND	GND	NA		38	GND	GND	NA	
39	HOOK0	PWR_GOOD	I	system	40	ITPCLK/HOOK4	Open	NA	
41	HOOK1#	BP_PWRGD_O	I	system	42	ITPCLK#/HOOK5	Open	NA	
43	VCC_OBS_AB	VCCIO_OUT	I	system	44	VCC_OBS_CD	VCCIO_OUT	I	system
45	HOOK2	PWR_DEBUG	O	processor	46	HOOK6	PLTRSTN#	I	system
47	HOOK3	PCH_SYS_PW	O	system	48	HOOK7/DBR#	DBR#	O	system
49	GND	GND	NA		50	GND	GND	NA	
51	SDA#	SDA	I/O	system	52	TDO	TDO	I	processor
53	SCL#	SCL	I/O	system	54	TRSTn	TRST#	O	processor
55	TCK1	Open	NA		56	TDI	TDI	O	processor
57	TCK0	TCK	O	processor	58	TMS	TMS	O	processor
59	GND	GND	NA		60	GND	GND (or XDP_PRESENT T# if required)	NA	

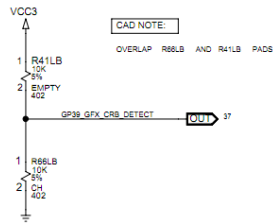
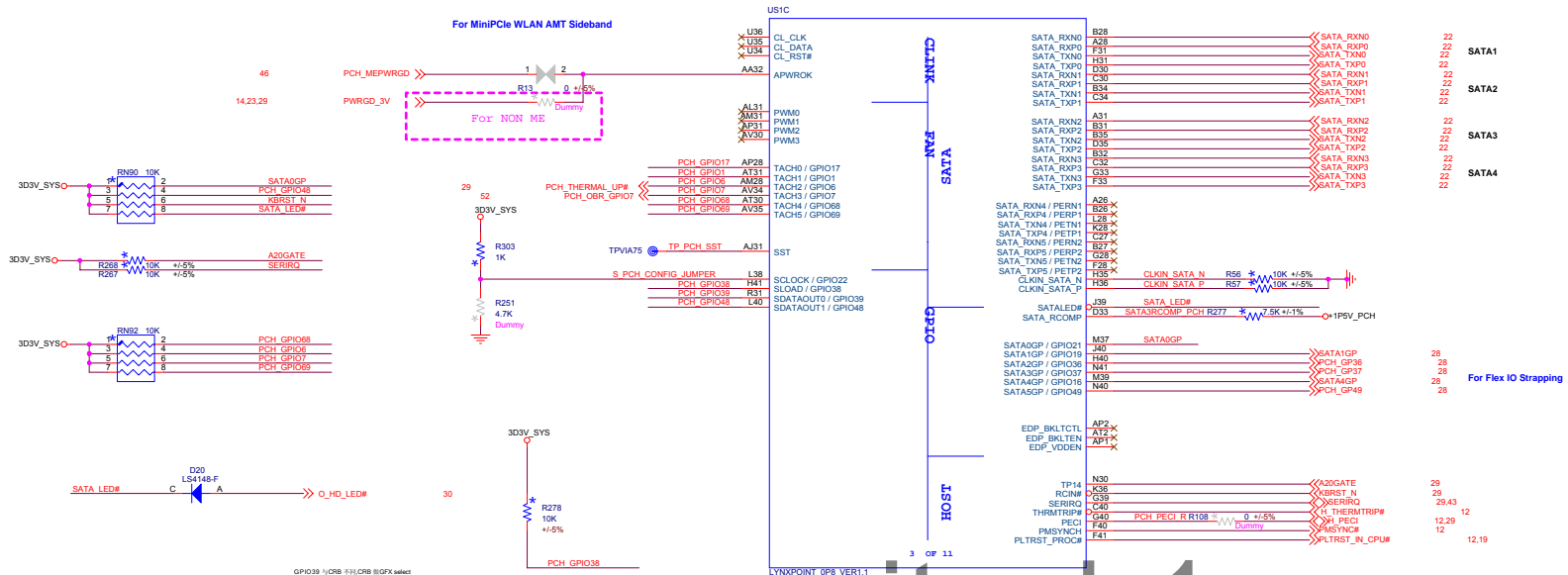
Table 4-1. PCH XDP Connector Pinout

Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	GND	GND	NA		2	GND	GND	NA	
3	OBSFN_A0	Open	NA		4	OBSFN_C0	GPIO8	I	PCH
5	OBSFN_A1	Open	NA		6	OBSFN_C1	GPIO35	I	PCH
7	GND	GND	NA		8	GND	GND	NA	
9	OBSDATA_A0	OC0# / GPIO59	I	PCH	10	OBSDATA_C0	SATA0GP / GPIO21	I	PCH
11	OBSDATA_A1	OC1# / GPIO40	I	PCH	12	OBSDATA_C1	SATA1GP / GPIO19	I	PCH
13	GND	GND	NA		14	GND	GND	NA	
15	OBSDATA_A2	OC2# / GPIO41	I	PCH	16	OBSDATA_C2	SATA2GP / GPIO36	I	PCH
17	OBSDATA_A3	OC3# / GPIO42	I	PCH	18	OBSDATA_C3	SATA3GP / GPIO37	I	PCH
19	GND	GND	NA		20	GND	GND	NA	
21	OBSFN_B0	Open	NA		22	OBSFN_D0	Open	NA	
23	OBSFN_B1	Open	NA		24	OBSFN_D1	Open	NA	
25	GND	GND	NA		26	GND	GND	NA	
27	OBSDATA_B0	OC4# / GPIO43	I	PCH	28	OBSDATA_D0	SATA4GP / GPIO16	I	PCH
29	OBSDATA_B1	OC5# / GPIO9	I	PCH	30	OBSDATA_D1	SATA5GP / GPIO49	I	PCH
31	GND	GND	NA		32	GND	GND	NA	
33	OBSDATA_B2	OC6# / GPIO10	I	PCH	34	OBSDATA_D2	GPIO18	I	PCH
35	OBSDATA_B3	OC7# / GPIO14	I	PCH	36	OBSDATA_D3	GPIO20	I	PCH
37	GND	GND	NA		38	GND	GND	NA	
39	HOOK0	RSRST#	I	PCH	40	ITPCLK/HOOK4	1.05V core#	NA	
41	HOOK1	BP_PWRGD_O	I	system	42	ITPCLK#/HOOK5	Open	NA	
43	VCC_OBS_AB	VccSus3_3	NA		44	VCC_OBS_CD	VccSus3_3	NA	
45	HOOK2	Open	I		46	HOOK6	PCH_PWROK	I	PCH
47	HOOK3	Open	NA		48	HOOK7/DBR#	SVS_RESET#	O	PCH
49	GND	GND	NA		50	GND	GND	NA	
51	SDA	I/O	system		52	TDO	JTAG_TDO	I	PCH
53	SCL	I/O	system		54	TRSTn	Open	NA	
55	TCK1	Open	NA		56	TDI	JTAG_TDI	O	PCH
57	TCK0	JTAG_TCK	O	PCH	58	TMS	JTAG_TMS	O	PCH
59	GND	GND	NA		60	GND	GND (or XDP_PRESENT T# if required)	NA	

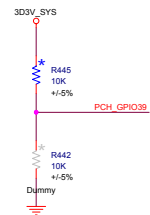




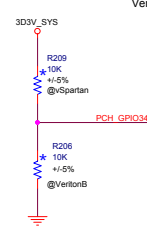
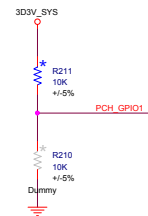
20120908 for Intel SBA Function, Need ME Power,Dummy R13  
R13 for NO\_ME Power APWROK connect PWROK\_3V



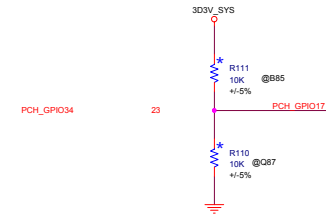
GFX SELECT TABLE	
GP39	GFX STYLE
0	NORMAL GFX
1	CUSTOMER GFX



Board ID



20121108 For BORAD ID  
vSpartan Stuff R209 Q87--Stuff R110 to 110 B85--Stuff R111 to 111  
VeritonB Stuff R206 Q87--Stuff R110 to 110 B85--Stuff R111 to 101

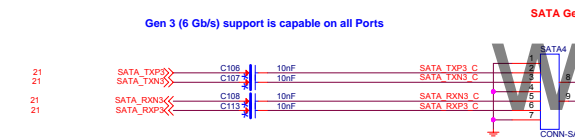
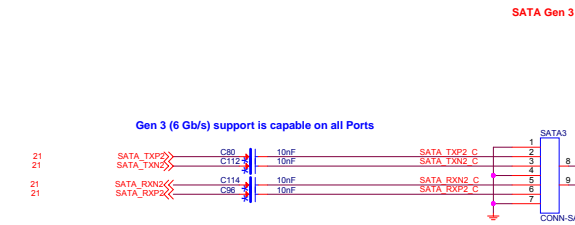
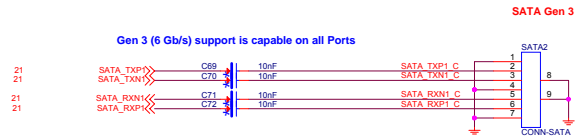
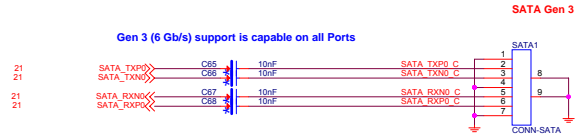


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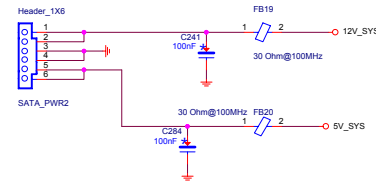
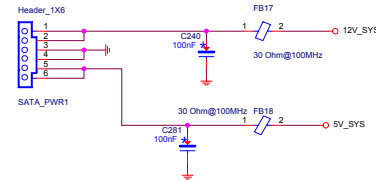


## SATA

20121108 SATA Footprint change to sata7\_sata3h84



20120828 SCH Review  
Delete SATA POWER 22uF&10uF for Bulk & EMC inefficacy  
FB double check with EMC  
20130607 FB17&FB19 Change to 5A for large power of ODD



20120903 for final POR, One sata power connector support two devices, delete SATA\_PWR3&4

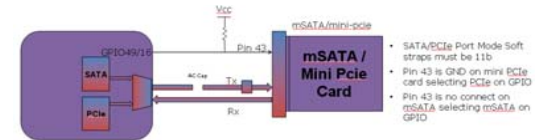
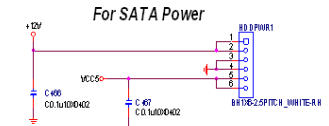


Table below summarizes the AC cap requirement on the motherboard when using SATA/PCIe mixed port.

Condition	PCIe only	SATA only	PCIe/SATA
PCH Tx	100 nF	10 nF	100 nF
PCH Rx	None	10 nF (Can be removed if choose NOT to support DC coupled ODDs)	None (put footprint and stuff with zero ohm for backup)

Figure 1: Schematic diagram of the input circuit for the ADXL345. The circuit shows three input lines: D3V\_SYS, +3V\_BATT, and V\_DUAL. D3V\_SYS is connected to R212 (10K) and D3V\_SYS. +3V\_BATT is connected to R244 (390KOhm) and DSW\_VR\_EN. V\_DUAL is connected to RN108 (10K Ohm) and SMDALERTW, SMDALERT#, and TMIN\_SHFT. All resistors have a tolerance of +/-5%.

Timing diagram for the A\_HDA\_RST# signal. The diagram shows the relationship between various signals and A\_HDA\_RST# over time. Signals include LPC\_A00, LPC\_A01, LPC\_A02, LPC\_A03, LPC\_D0[3:0], LPC\_FRAME#, A\_HDA\_BCLK, A\_HDA\_RST#, A\_HDA\_S0D\_0, FLASH\_OVERRIDE#, A\_HDA\_SYNC#, SPI\_MOSI, SPI\_MISO, SPI\_CS0, SPI\_CS#, SPI\_I02, and SPI\_I03. The A\_HDA\_RST# signal is shown as a blue waveform with a rising edge at approximately 31.32 ns. The FLASH\_OVERRIDE# signal is shown as a red waveform with a rising edge at approximately 27 ns. The A\_HDA\_SYNC# signal is shown as a red waveform with a rising edge at approximately 31 ns. The SPI signals are shown as red waveforms with rising edges at approximately 52 ns. The LPC signals are shown as red waveforms with rising edges at approximately 29.43 ns.

INTEGRATED 1.05V SUS VRM ENABLE  
SUS VRM ENABLED WHEN SAMPLED HIGH  
0 = DCPSUS1, DCPSUS2 and DCPSUS3 are powered  
from an external power source  
1 = Integrated VRMs enabled.

<b>DPWROK</b>	I	Connect to VccDSW3_3 power rail monitoring circuit on mother board. For platform not supporting deep sleep connect directly to RSMRST#. The DSW rails must be stable for at least 10 ms before DPWROK is asserted to PCH.
---------------	---	---

X1\_1  
Crystal Retainer

[illegible]

**GPIO8**  
This signal has a weak internal pull-up but requires an external pull down

303V\_SYS 303V\_SYS 303V\_SYS

R175 10K +5% R415 10K +5% R439 1K

RESERVE R439 FOR CRB  
STUFF R455 FOR HSW(DEFAULT)

Pin	MCU Pin	MCU Function	External Component	MCU Pin	MCU Function	External Component
32	C38	N32 PCH GPIO30		21	CP1 GPIO34	
31	C32	N32 PCH GPIO33				
30	C30	N34 PCH GPIO34				
29	C28	AC40 PCH GPIO8				
28	C26	AL40				
27	C24	AN22 PCH GPIO15				
26	C22	AC32 PCH GPIO15				
25	C20	AE34 PCH GPIO24				
24	C18	W41 PCH GPIO28				
23	C16	AL39 PCH GPIO28				
22	C14	W44 PCH GPIO28				
21	C12	CP10 CLKIN				
20	C10	P39 PCH GPIO18				
19	C8	P37 PCH SMI N				
18	C6	AC39 PCH GPIO25				
17	C4	W35 PCH GPIO26				
16	C2	AC36 PCH GPIO26				
15	C0	W32 PCH GPIO45				
14	C0	AC36 PCH GPIO45				
13	C0	AC40 PCH GPIO46				
12	C0	CP10 CLKIN				
11	C0	CP10 CLKIN				
10	C0	CP10 CLKIN				
9	C0	CP10 CLKIN				
8	C0	CP10 CLKIN				
7	C0	CP10 CLKIN				
6	C0	CP10 CLKIN				
5	C0	CP10 CLKIN				
4	C0	CP10 CLKIN				
3	C0	CP10 CLKIN				
2	C0	CP10 CLKIN				
1	C0	CP10 CLKIN				
0	C0	CP10 CLKIN				

[illegible]

3.0V\_DSW

R317 1K

R517 10K +/-5%

R512 10K +/-5%

R355 10K +/-5%

R315 1K

R422 10K +/-5%

R397 10K +/-5%

R457 1K

R213 10K +/-5%

R417 10K +/-5%

PCIE\_WAKE\_UPI

PCIE\_GP1045

S\_SUSWARM

LAN\_WAKE\_N

PCIE\_GP1072

PCIE\_GP1045

PCIE\_GP108

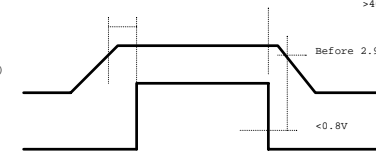
PCIE\_GP1018

PCIE\_RSMRST1

Figure 10 shows the pin connection for the RN96 10K resistor. The resistor is a 10K Ohm resistor. The connections are as follows:

- Pin 1: 3D3V\_ALW
- Pin 2: SUS\_STAT# PCH
- Pin 3: SLP S5#
- Pin 4: PCH\_GPIO44
- Pin 5: Ground
- Pin 6: Ground
- Pin 7: Ground
- Pin 8: Ground
- Pin 9: Dummy

The diagram shows a voltage divider circuit enclosed in a dashed blue box. The input is  $V_{SM}$  connected to a resistor  $R64$  with a value of  $1.8K$ . This resistor is connected to a node that branches to a resistor  $R234$  with a value of  $3.3K$  and a tolerance of  $\pm 1\%$ . The other end of  $R234$  is connected to ground. A red line labeled  $DRAM\_PWGRD\_C$  is connected to the node between  $R64$  and  $R234$ . The text **PDG 0.7** is written vertically on the left side of the box.

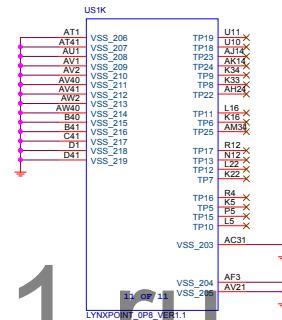
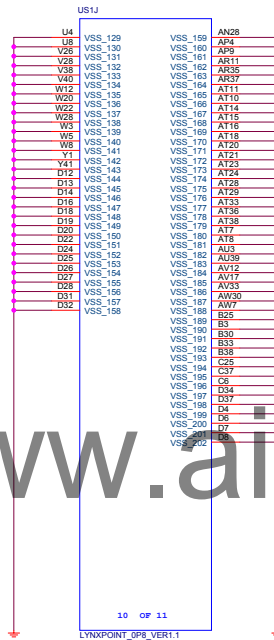
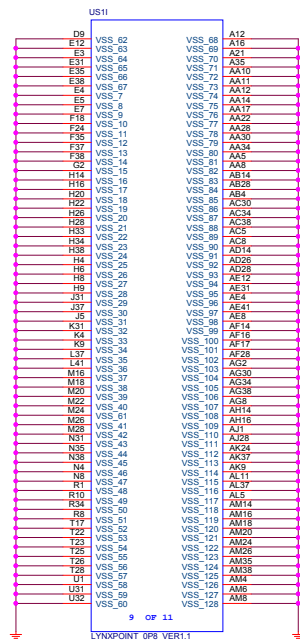






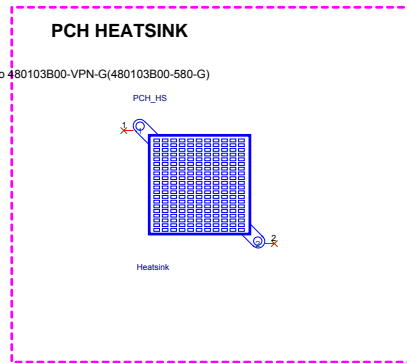






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20120907 for layout request  
PCH Heatsink 48010WH00-23C-G change from to 480103B00-VPN-G(480103B00-580-G)



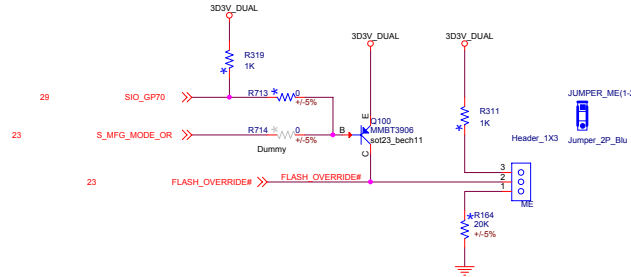
## ME Disable (Flash override)

MFG\_Mode move to GP38

20120824 For BIOS Request add GPIO34 from SIO control ME

20120922 for Intel ME Request  
ME GPIO Change to 3D3V\_DUAL

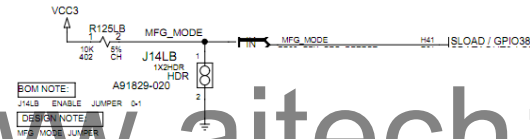
20121124 Stuff R713,Dummy R714,Add SIO GP70(SIO\_GP70) pull high resistor R319 to 3D3V\_DUAL  
Change R310 from 1K to 0ohm for software control ME disable



20121126 Change ME header to HW control  
ME\_DISABLE 3-pin  
1-2: NORMAL  
2-3: ME DISABLE

If high disable ME

HDA\_SDO  
0 = Enable security measures defined in the Flash  
Descriptor.  
1 = Disable Flash Descriptor Security (override)



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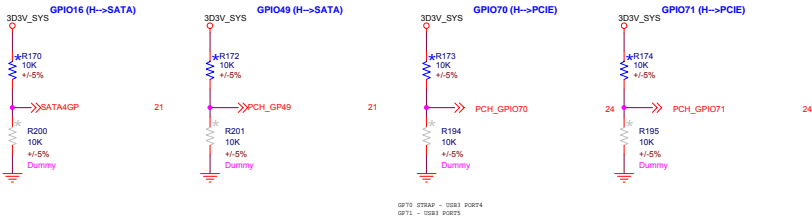
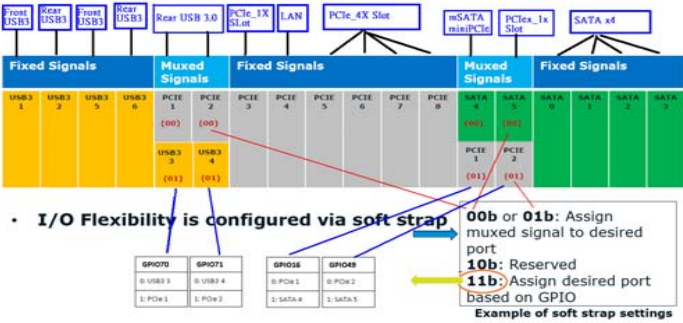
Support Intel vPro and AMT 9.0.Reserved AMT CONN  
Intel APS, or Automatic Power Switcher, is a tool that interfaces with  
the Intel Platform Enablement Test Suite (PETS) used to test  
compliance to Intel ME requirements and is a validation vehicle to  
assist with the reproduction of power management and power  
sequencing issues. The APS signals are required to be present at an  
accessible location on the board

Table 22-6. Automatic Power Switcher (APS) Connector (aka PETS Connector)

Pin	Signal Name	Description
1	VccSus3_3	3.3 V Suspend Power Well
2	SLP_S3#	When asserted (0) system is in S3
3	VccDSW3_3	Used to determine if system is in Deep S3
4	SLP_S5#	When asserted (0) system is in S5
5	SLP_S4#	When asserted (0) system is in S4
6	SLP_A#	When asserted (0) Intel ME is in Mof
7	+V3.3DS	Used to determine if the system is in Deep S4/S5
8	GND	Ground
9	RTCRST#	When asserted (0) CMOS is cleared
10	GND	Ground for RTCRST#
11	PWRBTN#	When asserted (0) Power Button Pushed
12	GND	Ground for PWRBTN#
13	SYS_RESET#	When asserted (0) Reset Button Pushed
14	GND	Ground for SYS_RESET#

Lynx Point I/O Flexibility

- New architecture allows some I/O Ports to be configured at time of system design



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No Reboot Mode

SPKR (IN-PD)	Description
High	No reboot mode: Enable
Low	No reboot mode: Disable

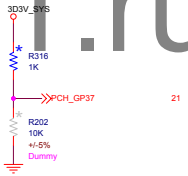


20121108 Shift R325 for HW Straps same as GRB

TLS Confidentiality

GPIO37 (IN-PD)	Description
High	ME Crypto TLS cipher suite with confidentiality
Low	ME Crypto TLS cipher suite with no confidentiality

DEFAULT

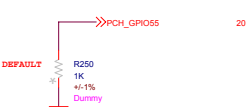


DMI AC COUPLING FULL VOLTAGE MODE WHEN SAMPLED LOW



Topblock Swap Mode

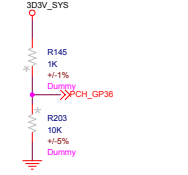
GPIO55 (IN-PD)	Description
High	Topblock swap mode: Disable
Low	Topblock swap mode: Enable



20

DMI Rx Termination

GPIO36 (IN-PD)	Description
Low	DMI Rx Termination Voltage



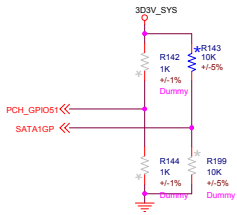
21

Boot BIOS Destination Selection

GPIO51 (IN-PD)	SATA1GP/GPI9 (IN-PD)	Description
Low	Low	Flash cycle routed to LPC
High	Low	Flash cycle routed to PCI
High	High	Flash cycle routed to SPI

20

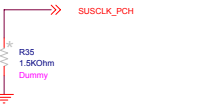
21



On-Die PLL Voltage Regulator

GPIO62/SUSCLK (IN-PD)	Description
High	Regulator is enabled.
Low	Regulator is disabled.

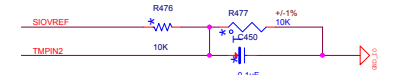
DEFAULT



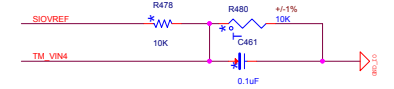
23

WEAK INTERNAL PULLUPS ON GP51. DEFAULT SPI BOOT DEVICE

## SYSTEM TEMPERATURE



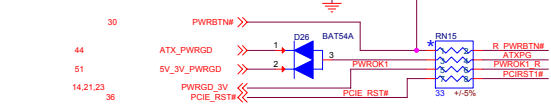
## VRD TEMPERATURE



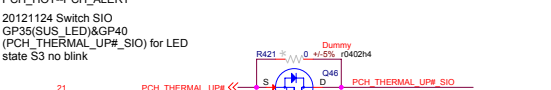
20121116 Dummy 3D3V\_5V\_SB\_CTL signal  
pull high resistor R506 for UP7536&7537 EN  
pin internal pull high



20120828 ATX\_PWRGD&  
5V\_3V\_PWRGD 起控制SIO  
ATXPG,其发出PWRGD\_3V

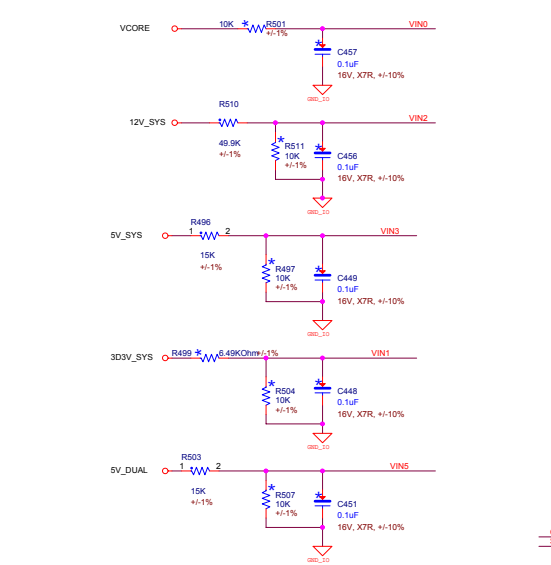


20120825 Therm shutdown--SIO\_GP10.SMI  
PCH\_PME--PCH\_GPIO13.SMI  
PCH\_HOT--PCH\_ALERT



20120912 Follow ITE VIN分压线路

20121108 Change R510 to 49.9K,R496 to 15K,R503 to 15K for HW monitor OV~2.8V

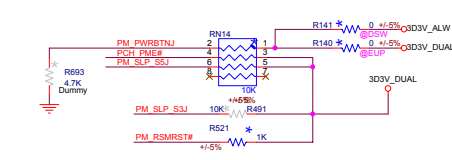


20120908 For ITE Check  
VIN1~3D3V\_SYS VINS~5V\_DUAL  
因DSW时通过VINS检测5V\_DUAL

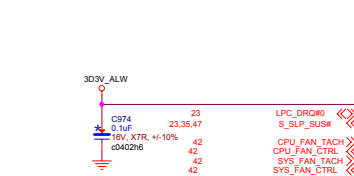
20120912 Add Q41防S4 S5时5V\_DUAL漏电

20120918 Remove Q41 for SIO Vendor check  
DSW 是不会漏电

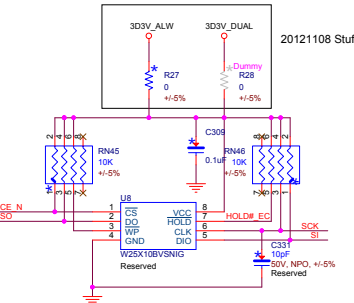
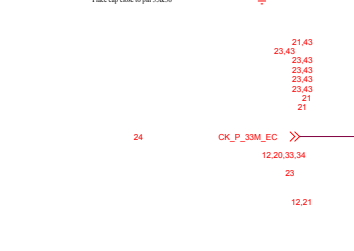
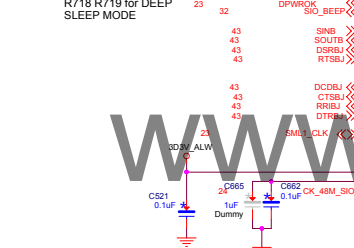
20121108 PM\_RSMRST# pull high resistor R521 change to 1K for RSMRST level



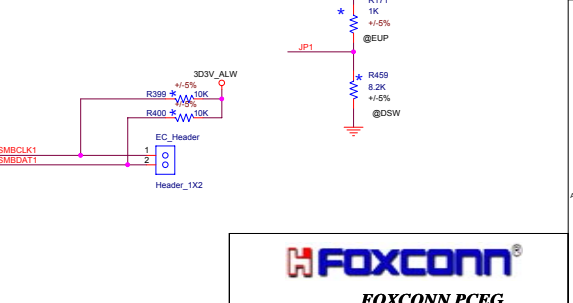
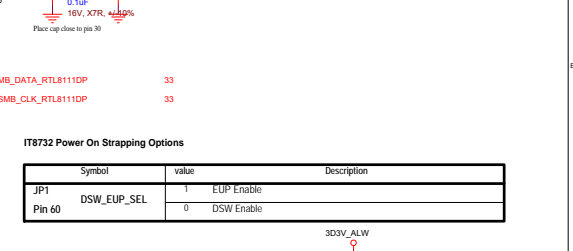
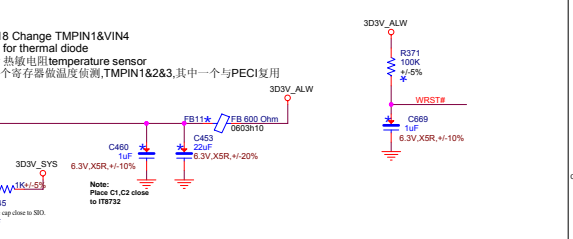
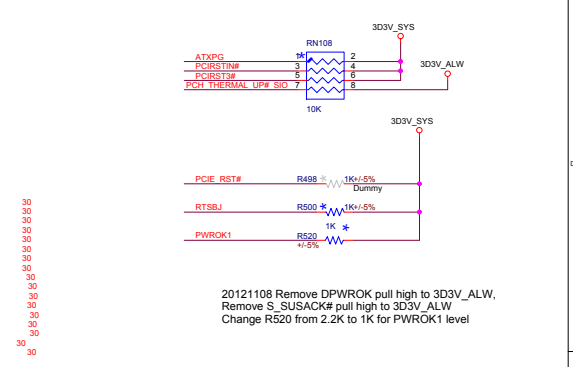
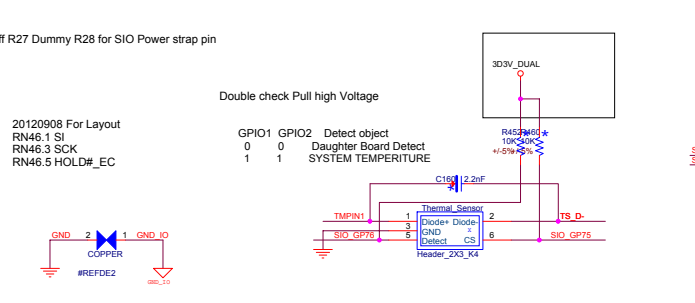
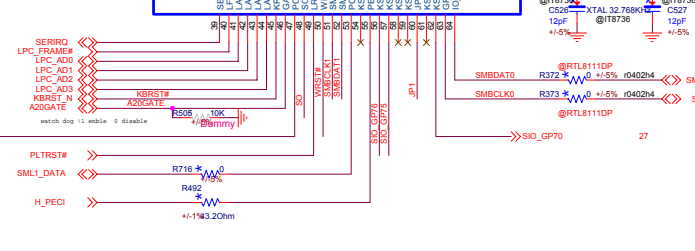
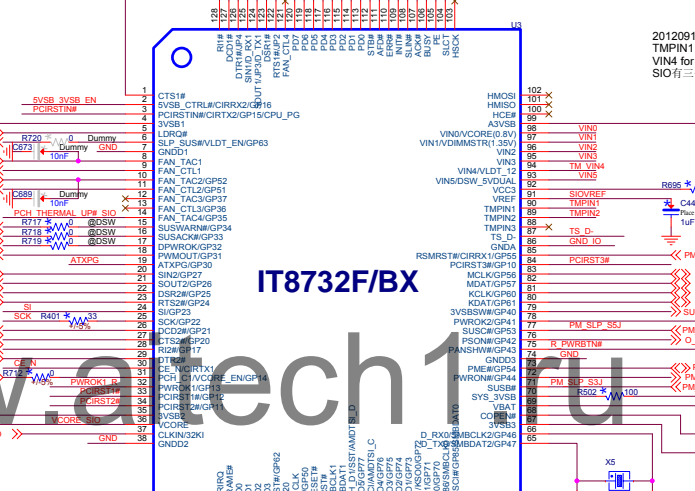
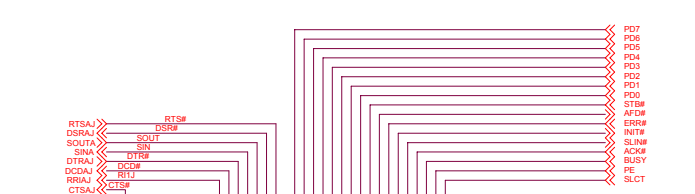
20121108 DEL C657 for EUP sequence



20120825 Stuff R717  
R718 R719 for DEEP  
SLEEP MODE

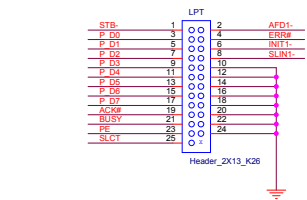
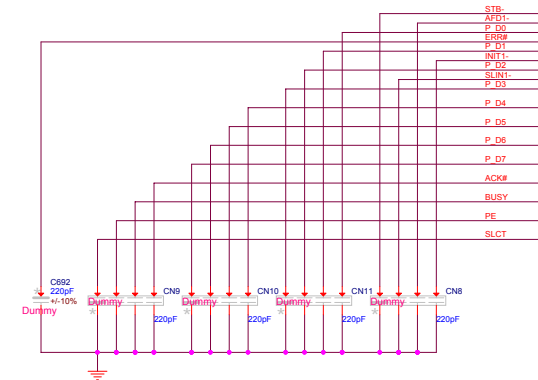
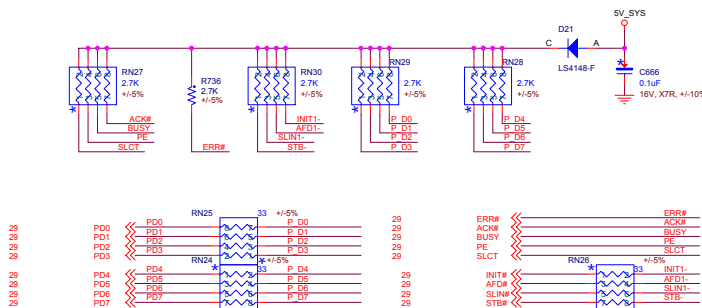


20120830 SIO Return  
1.本用到DSW JP1 需pull high,当pull low时改为680ohm--R459 680ohm  
2.Pin2(VSUS\_CTL)在开EUP进S5时High,S0/S3/S4时为Low,外部线路请确认  
3.Pin3(PCIRSTIN)请Pull high,no floating--RN108.3 to 3D3V\_SYS  
4.做DSW请预留Pin6(SLP\_SUS#)到南桥--R720 Dummy  
5.S\_SUSWARN#(R512) Pull只做预留--改在PCH端Pull high,PCH有要求  
6.Pin19 ATXPG差5V,可直接给IO  
7.Pin31/Pin53 只能做读取PCH的温度,请确认  
8.Pin75 Button(C413建议改1uF),串联电容建议靠近IO端  
9.PCIRST3非Push Pull,请Pull high, PCIRST1(R498)可只做预留--R165 to 3D3V\_SYS,R498 Dummy  
10.Temp3如做Thermal Diode检测时,Diode负载需靠近Pin87/TS\_D-  
11.做DSW时 5V\_DUAL需给Pin9(VINS)做检测,VIN分压电阻值请参考ITE线路  
12.开EUP时,R1可通过PCH做(Wake Up)请确认--R1 Eup 不做WakeUp

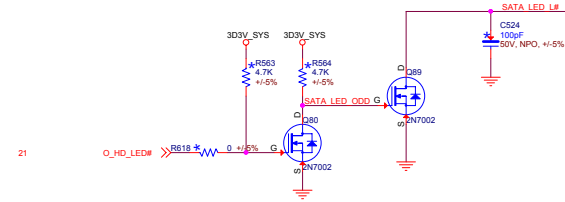


## LPT PORT

## Front Panel Connector

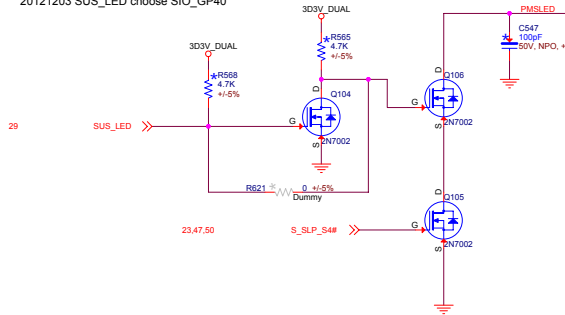


Front Panel Switch/LED			
HDD_LED+	1	2	Power
HDD_LED-	3	4	Power LED(Green)
GND	5	6	Power Button
Reset button	7	8	Detect pin
RSV	9	10	Key
Unused	11	12	LAN_LED+
Unused	13	14	LAN_LED-



20120825 SUS\_LED choose SIO\_GP35

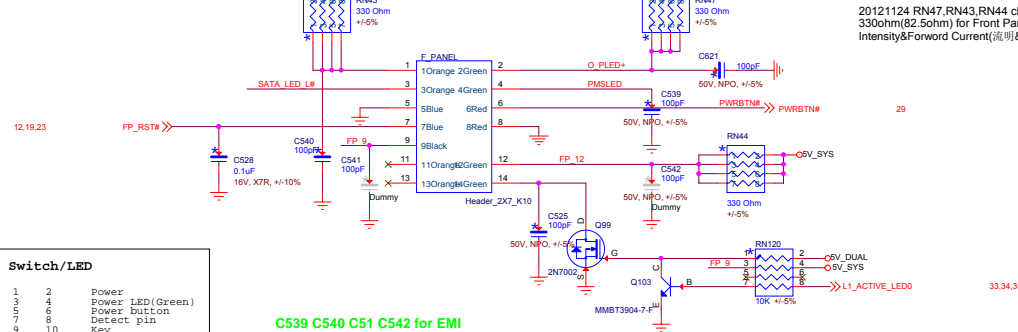
20121203 SUS\_LED choose SIO\_GP40



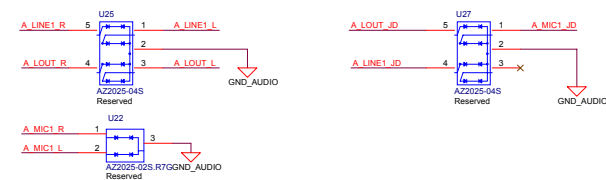
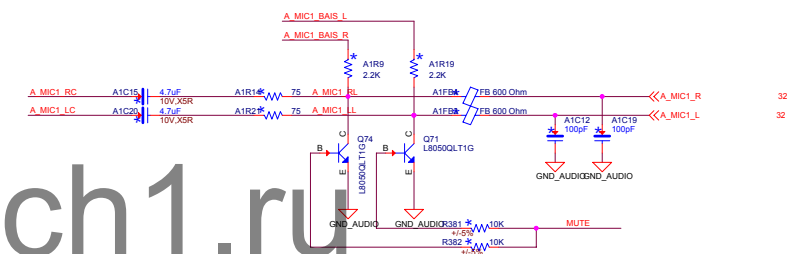
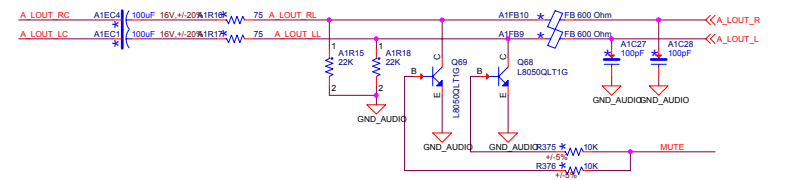
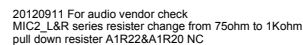
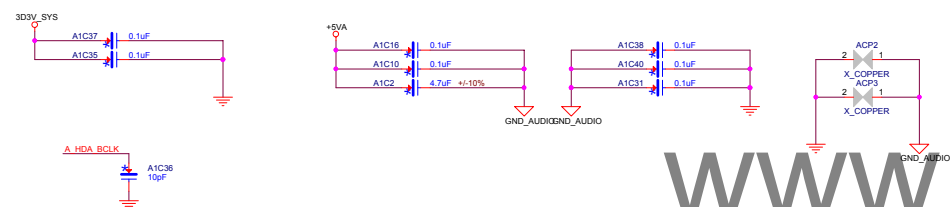
Power LED

State	SUS_LED	Colour
S0	0	Always ON
S3/S4	1	Blinking
S5	1	OFF

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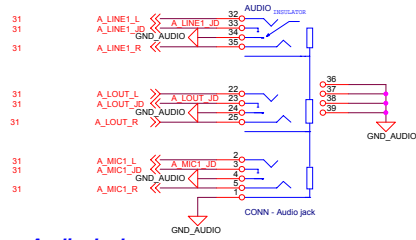


20121124 RN47,RN43,RN44 change to 330ohm(82.5ohm) for Front Panel LED Luminous Intensity&Forward Current(流明&电流强度)



Q57 Q58 Q66 Q67 Q68 Q69 For ACER EE Request Audio de-pop circuit  
U22 U25 U26 U27 U32 U35 TVS protection for audio

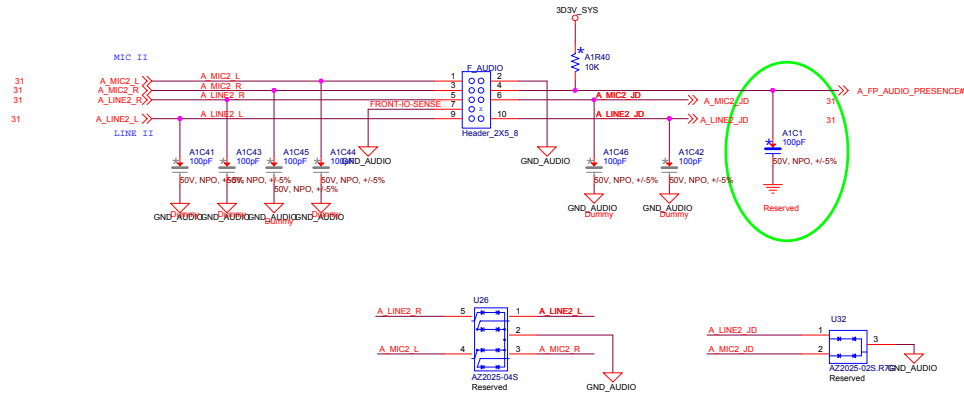
## Audio Jack



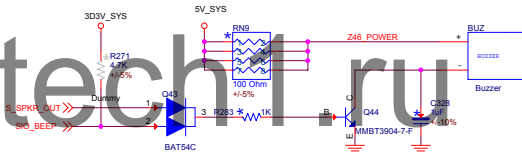
### Audio Jack

- C LINE IN (UAJ)
- B LINE OUT (UAJ)
- A MIC IN (UAJ)

## Front\_Audio

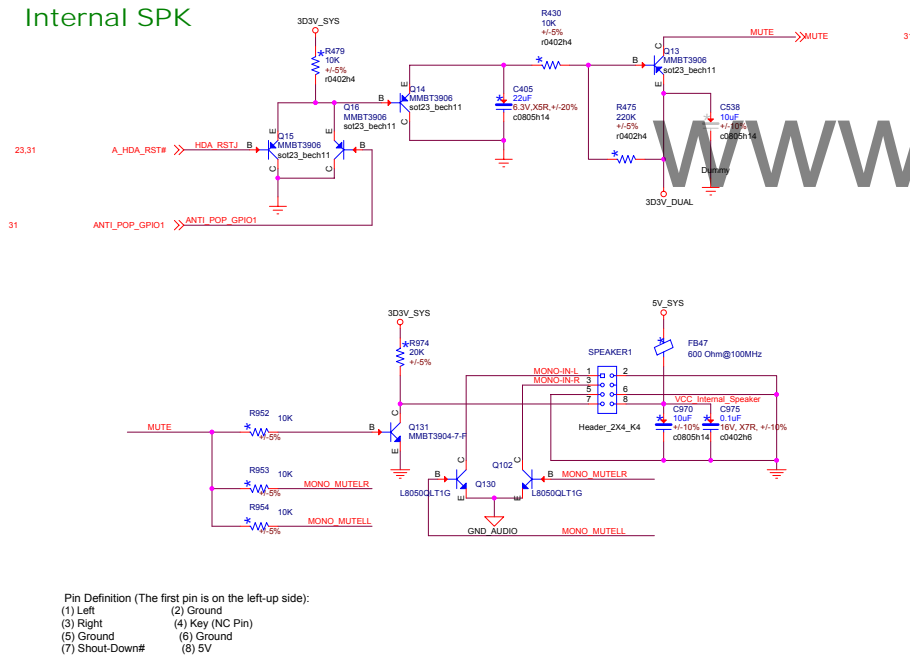


## BUZZER



20120828 check S\_SPKR\_OUT&SIO\_BEEP Default state

## Internal SPK



Pin Definition (The first pin is on the left-up side):

- (1) Left
- (2) Ground
- (3) Right
- (4) Key (NC Pin)
- (5) Ground
- (6) Ground
- (7) Shout-Down#
- (8) 5V

20120827 Internal SPK GND same as Audio Jack



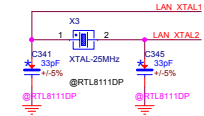
AUDIO CONN/SPDIF		
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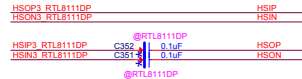
## PCIE LAN Chipset

2020906 RTL8111DP Crystal change from 25MHz +/-20ppm to 25MHz +/-30ppm

$$C1=C2=2CL-(C8+C1)$$
$$C1=C2=2*20-(7+2)=31$$



### LAN PCIE



### LAN CLK



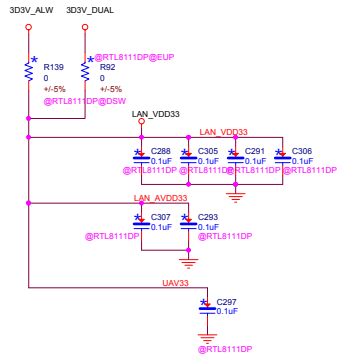
**SMBus-PCH** 20121108 Change R432 from shortpad to 0ohm resistor for ALERT wakeup(auto restart)



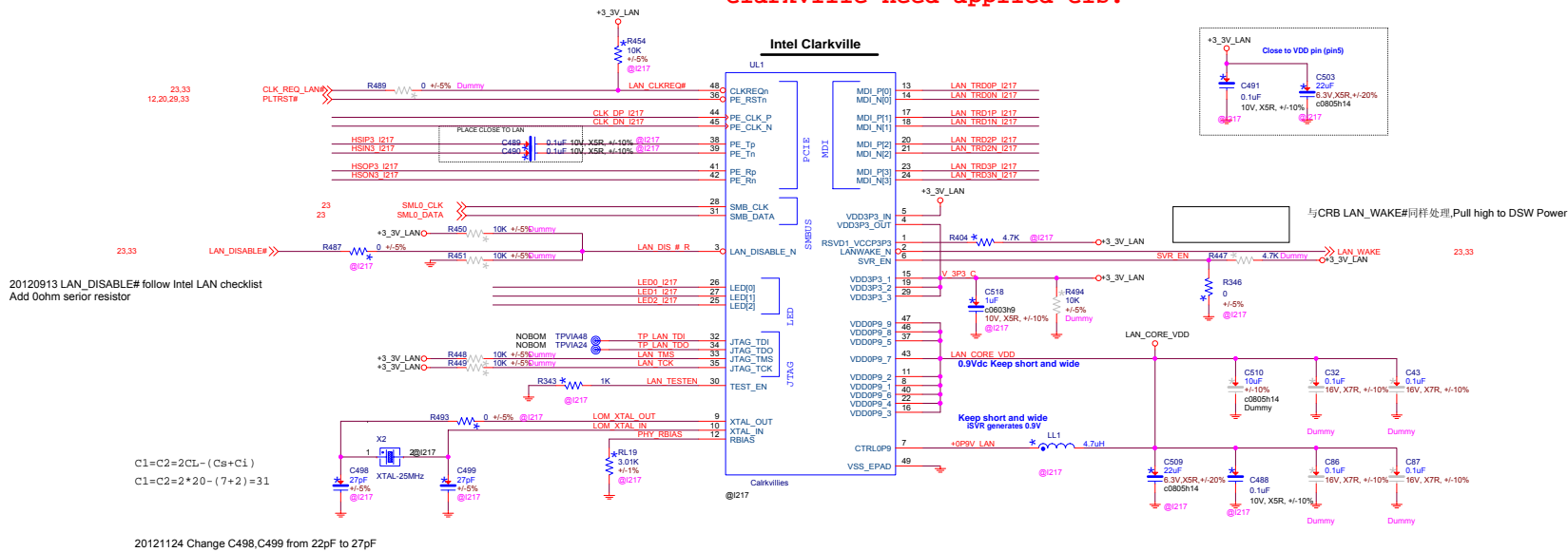
### SMBus-SIO



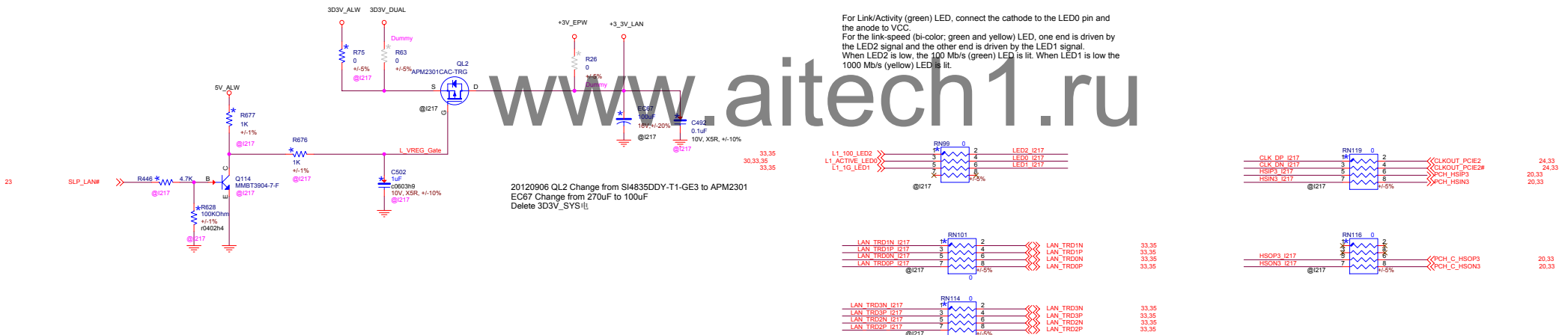
20120911 SMBus connect from PCH to DASH. Pull high resistor need 1K. PCH source change from 2.2K to 1K. Delete DASH pull high



# Clarkville need applied CIS.



For Link/Activity (green) LED, connect the cathode to the LED0 pin and the anode to VCC.  
For the link-speed (bi-color; green and yellow) LED, one end is driven by the LED2 signal and the other end is driven by the LED1 signal.  
When LED2 is low, the 100 Mb/s (green) LED is lit. When LED1 is low the 1000 Mb/s (yellow) LED is lit.



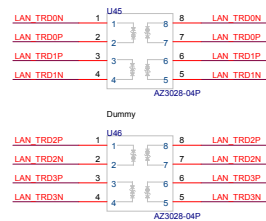
20120915 Acer EE Request  
LED1--Active  
LED2--Speed

LED0--Active  
LED1--Yellow  
LED2--Green

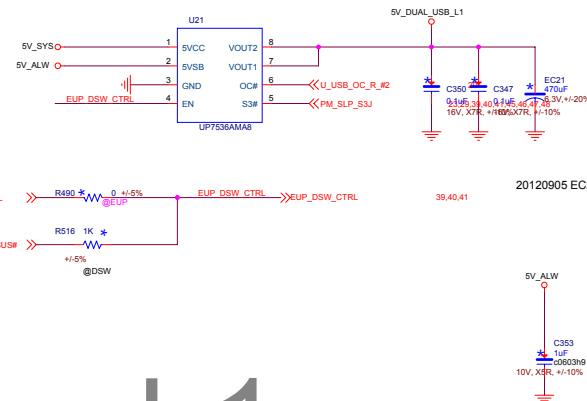
When LED2 is low, the 100 Mb/s (green) LED is lit. When LED1 is low the 1000 Mb/s (yellow) LED is lit.



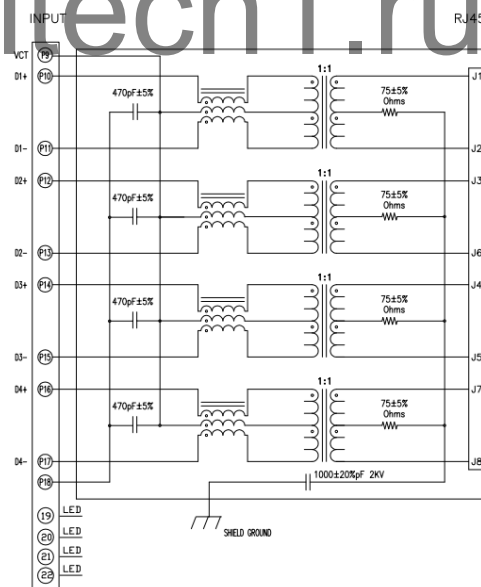
20120907 for layout request  
RN153.8 RN153.6 swap  
L33.5 L33.6 swap



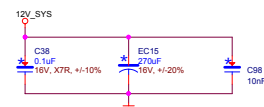
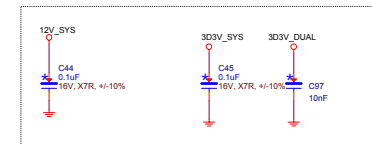
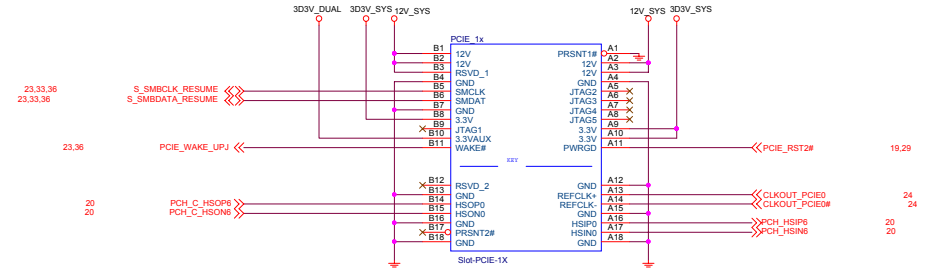
Traces or surface shapes from VCC to the thermistor, to CBYPASS and to the connector, Power and ground pins should be at least 50 mils wide. Power and ground nets should have double vias. Trace lengths should be kept as short as possible.



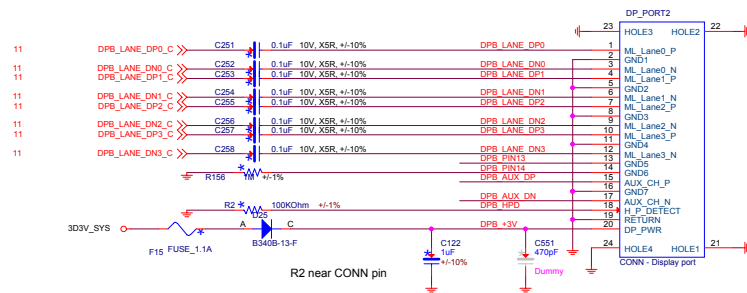
20120905 EC21 Change from 270uF to 470uF



## PCIE 1X

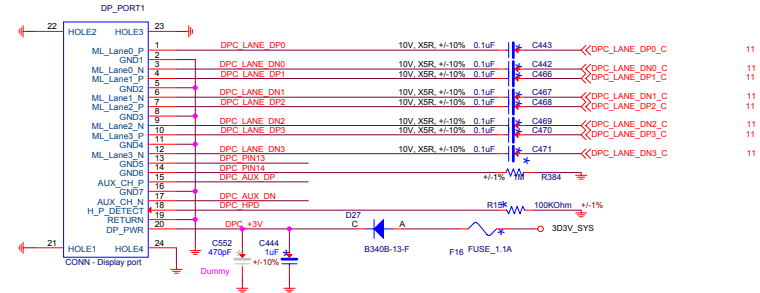


## 2\* Display Port

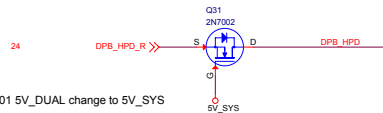


D25 for ACER EE Request Leakage Current Protection  
F15 for Over Current Protection

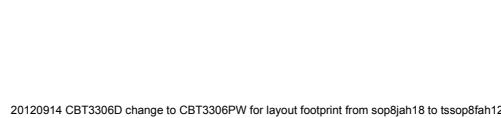
20121108 Change D25&D27 from 0.35A to 3A for OC



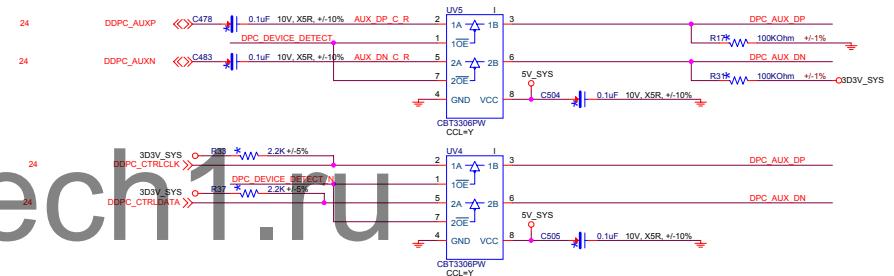
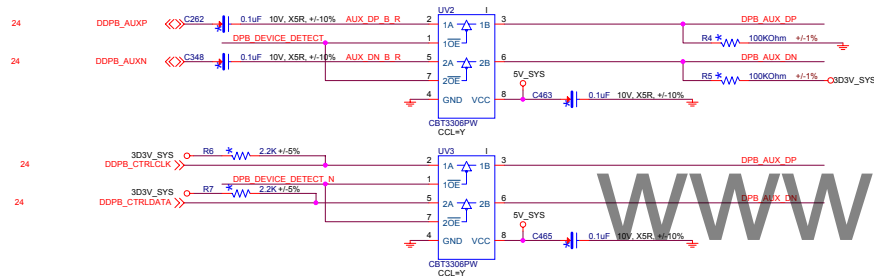
Pin13--GND in DP mode and Cable Adaptor Detect (CAD) in DP ++, DVI and HDMI Modes.  
Pin14--GND in DP and DVI modes and is Consumer Electronics Control (CEC) in HDMI mode.



20120901 5V\_DUAL change to 5V\_SYS

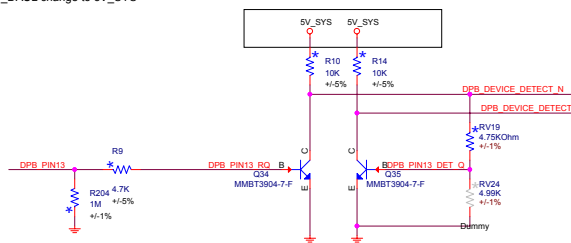


20120914 CBT3306D change to CBT3306PW for layout footprint from sop8jah18 to tssop8fah12

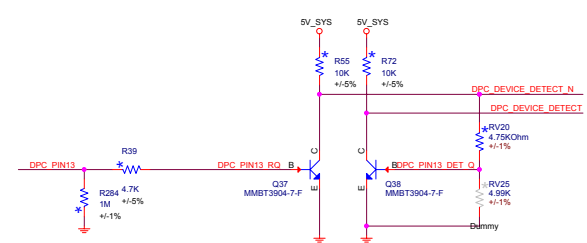


20120908 5V\_DAUL change to 5V\_SYS

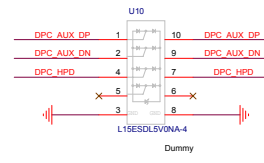
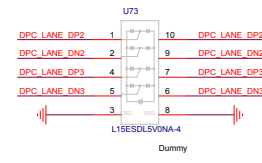
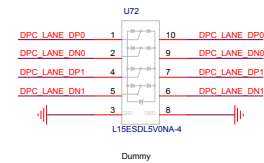
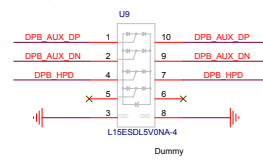
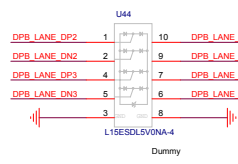
PIN13	DEVICE_DETECT	DEVICE_DETECT_N	FUNCTION
L	L	H	DP
H	H	L	DONGLE



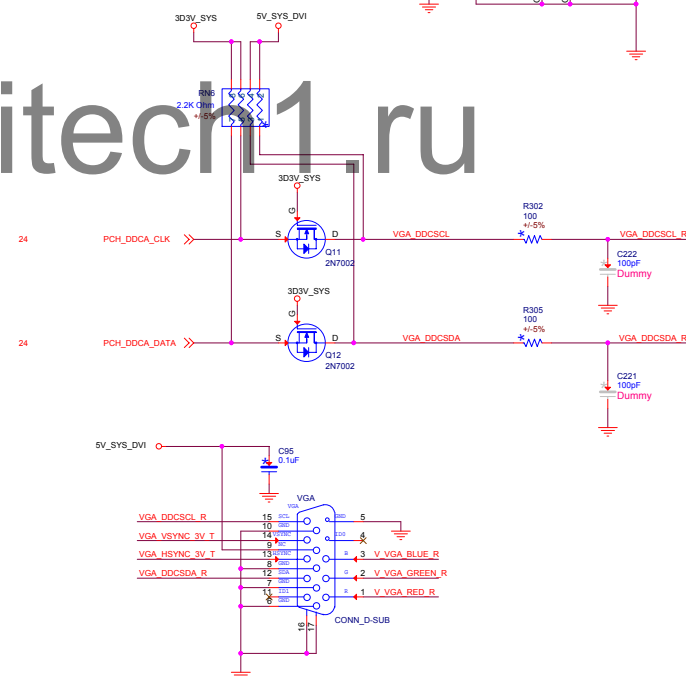
PIN13		FUNCTION
DP	DONGLE	
L	X	DEVICE_DETECT
X	H	DEVICE_DETECT_N



20120912d change AUX ESD from IP4220CZ6 to L15ESD  
減少容抗



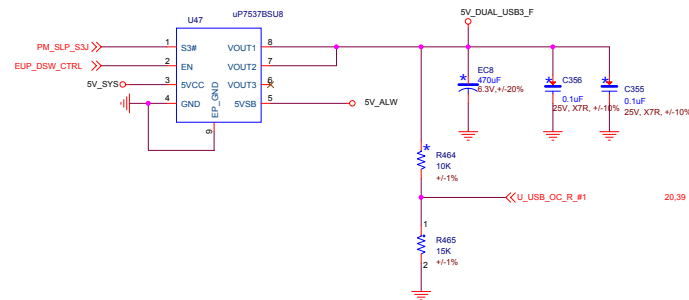
20120903 For Layout Request  
RN128.1pin 3pin swap  
RN128.5pin 7pin swap  
RN127.5pin 7pin swap



Title			
DVI-D&VGA			
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CURRENT-LIMIT AND SHORT-CIRCUIT PROTECTIONS						
$I_{LIM}$	Current Limit Threshold	APL3510A/B, APL3511A/B, $V_{IN}=2.7V$ to $5.5V$ , $T_A=-40 \sim 85^\circ C$	2.1	2.5	2.9	A
		APL3510C/D, APL3511C/D, $V_{IN}=2.7V$ to $5.5V$ , $T_A=-40 \sim 85^\circ C$	1.1	1.5	1.9	A

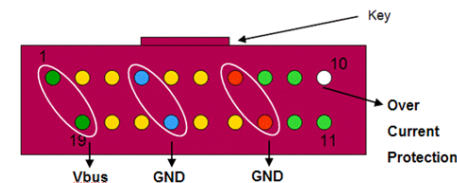
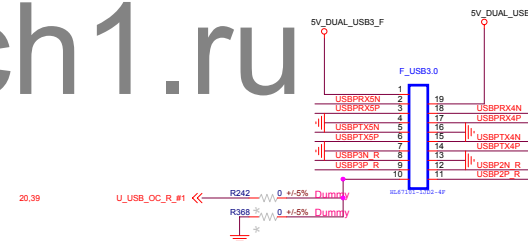
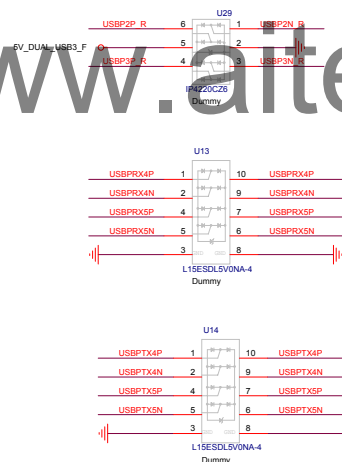
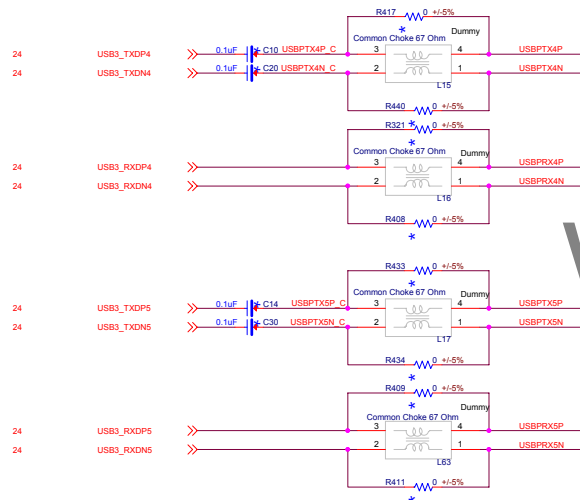
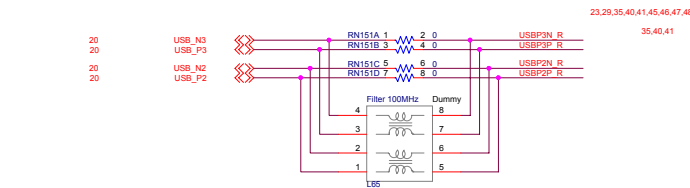
20121108 No connect Vout3 pin6 for UP7537 over current protect



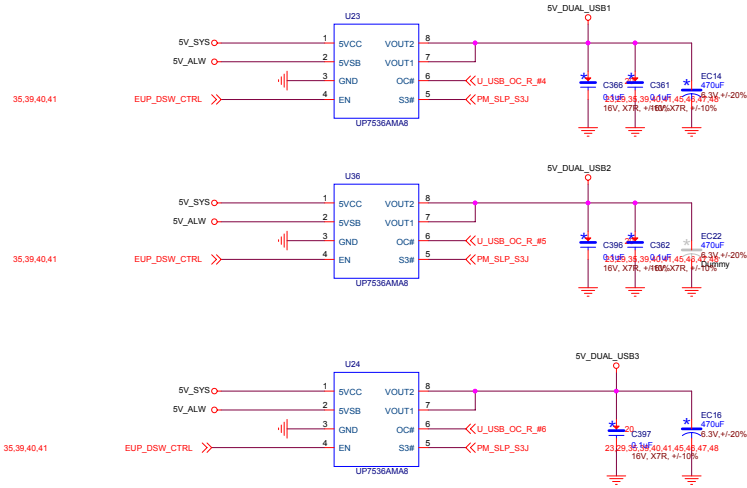
Make the power-carrying traces wide enough that the system fuse blows on an overcurrent event. If the system fuse is rated at 1 A, then the power-carrying traces should be wide enough to carry at least 1.5 A

For each USB3.0 Current 0.9A,

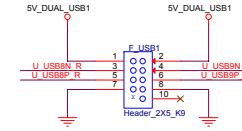
20120829 USB POWER IC change to UP7537



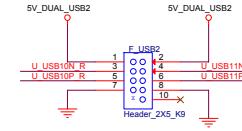
20121108 OC pin--active low,open-drain output



20120827 USB OC IC Change to UP7536  
 20120903 for layout request EC16 change from 270uF DIP0811 to 470uF DIP0611,  
 2020905 EC14 EC22 EC16 Dummy  
 EC22 EC16 Change from 270uF to 470uF  
 20121121 Stuff EC14&EC16 for USB2.0 device

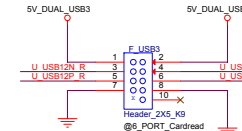


Port10&11 change to Cardread

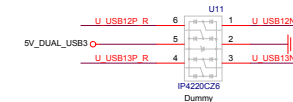
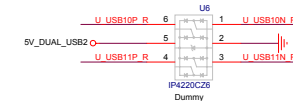
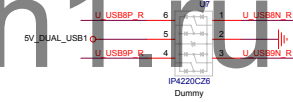
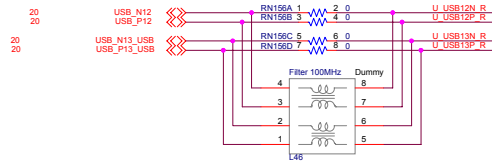
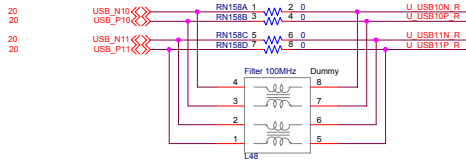
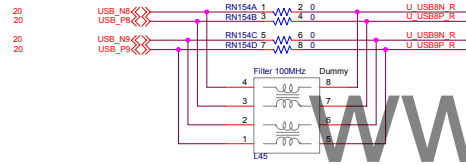
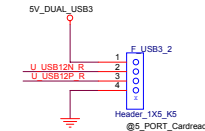


20121116 For latest POR  
 Change F\_USB2 to Cardread Q87&B85,F\_USB3 to USB device

Port12&13 For USB device



20121124 F\_USB3\_2 HH P/N confirm



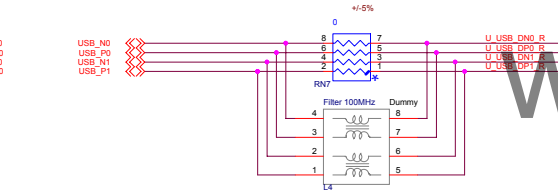
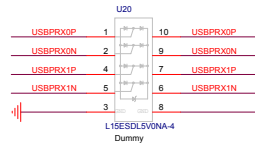
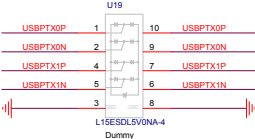
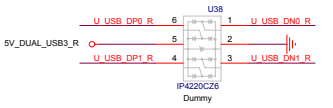
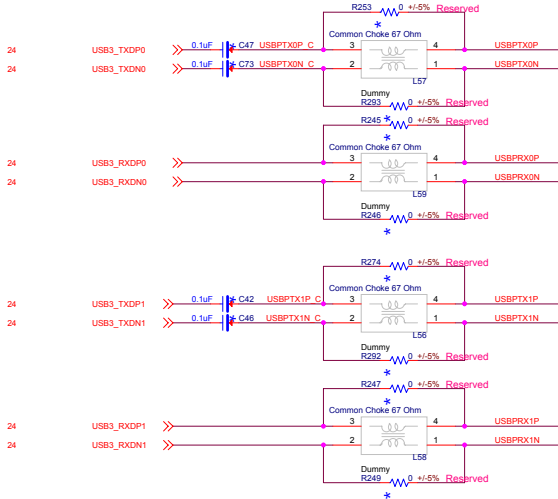
Title			
USB2.0 Header			
Size	Document Number	Rev	
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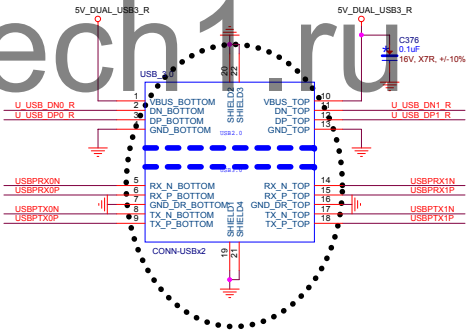
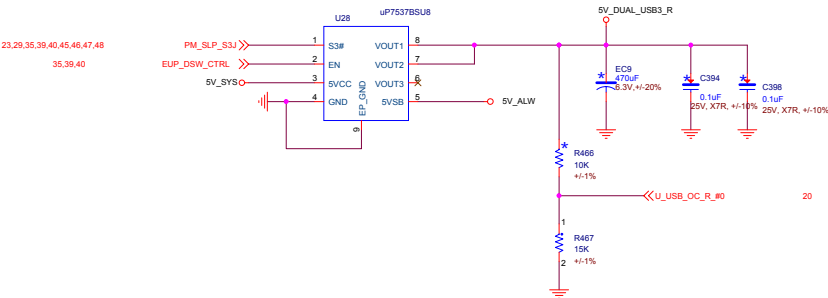
Rear USB3.0 \*2

20120904 for layout request  
U19 6pin 7pin swap 4pin 5pin swap  
L57 1pin 4pin swap 2pin 3pin swap

20120829 USB3.0 ESD change to IP4220CZ6 for 2.0 signal & L15ESDL5V0NA-4 for 3.0 signal

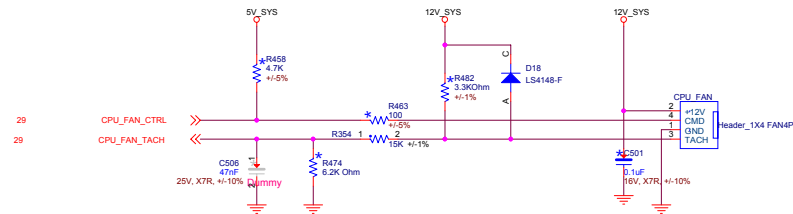


20121108 No connect Vout3 pin6 for UP7537 over current protect

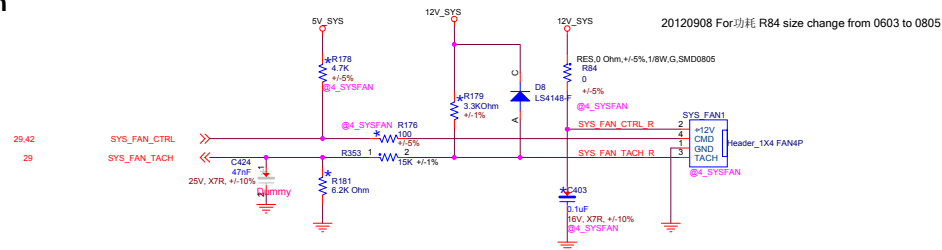
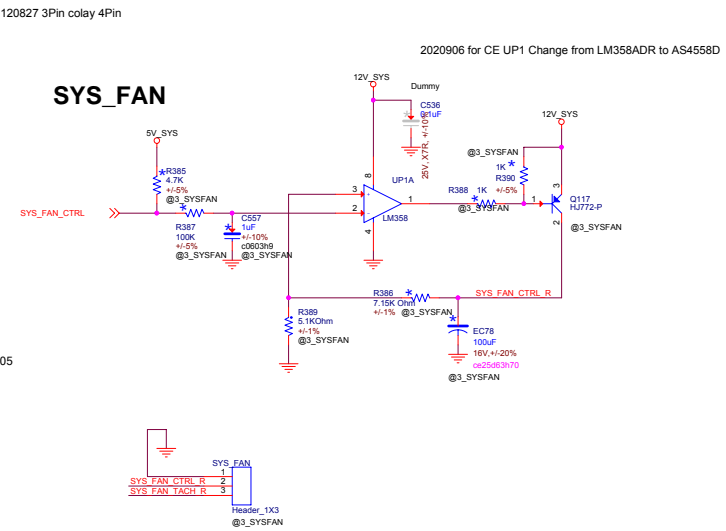


20120827 USB2.0 Colay delete

## CPU Fan

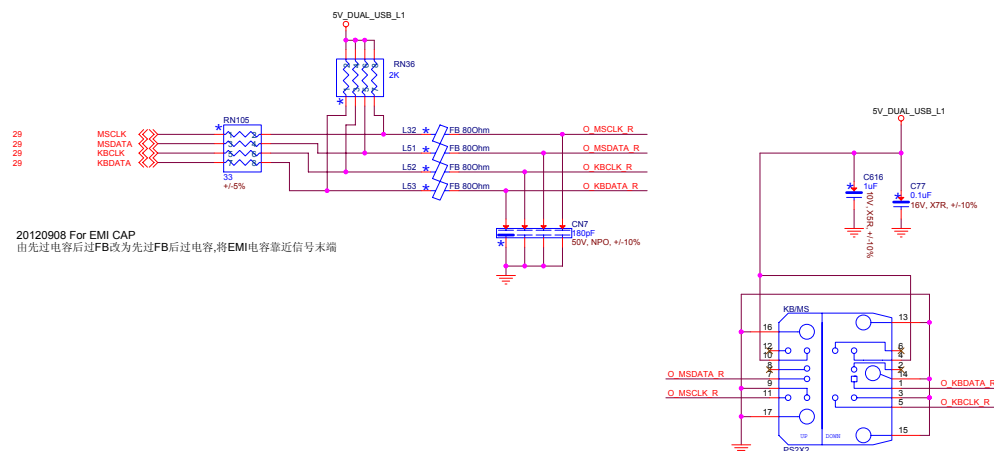


**SYS Fan**

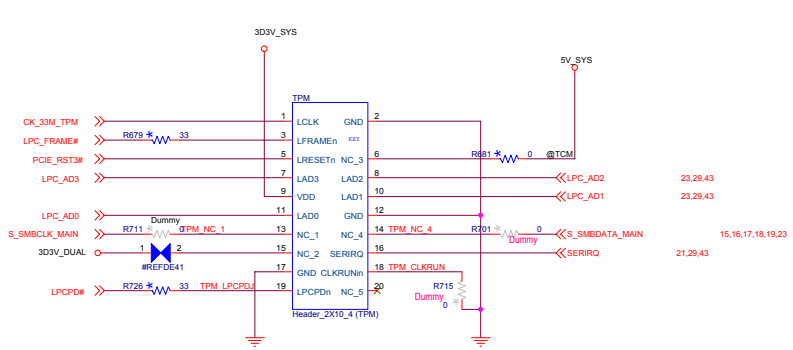
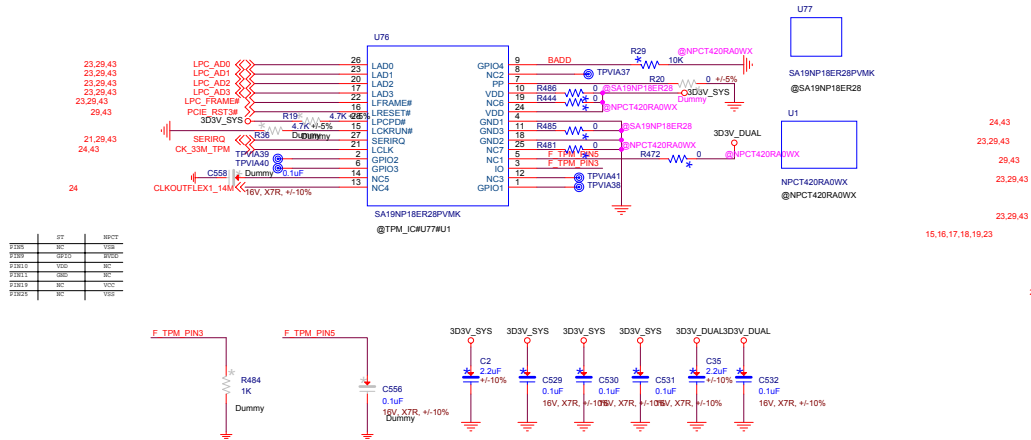
**SYS\_FAN**

[www.aitech1.ru](http://www.aitech1.ru)

**KB /MS CONN**



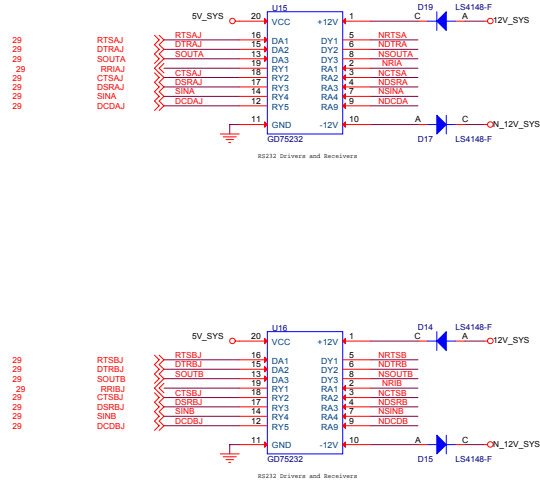
20120912 TPM IC from SLB9635T change to ST19NP18ER28



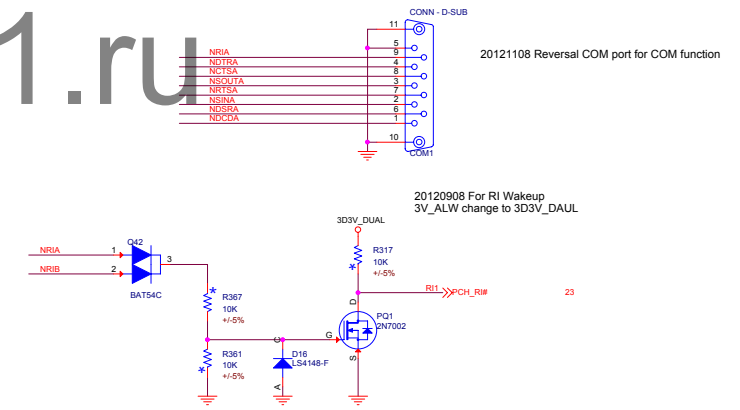
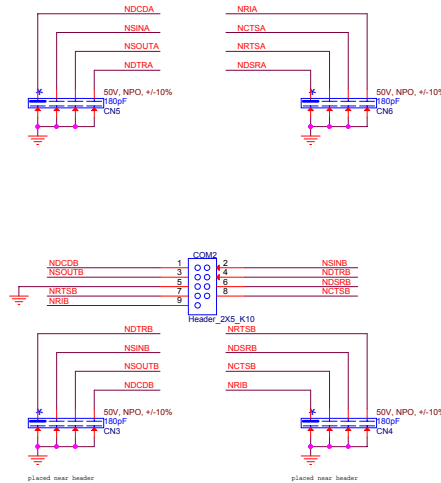
20120827 Add TCM Function for Fangzheng



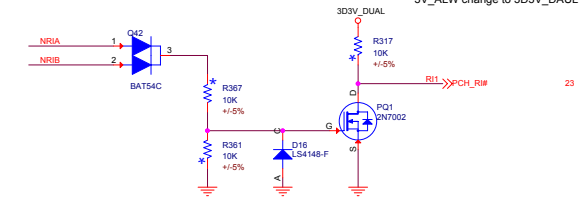
20120828 RIA&RIB through levelshift control PCH\_RI,through GD75232 control SIO



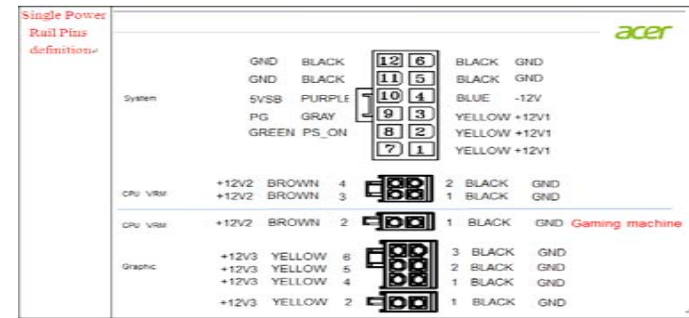
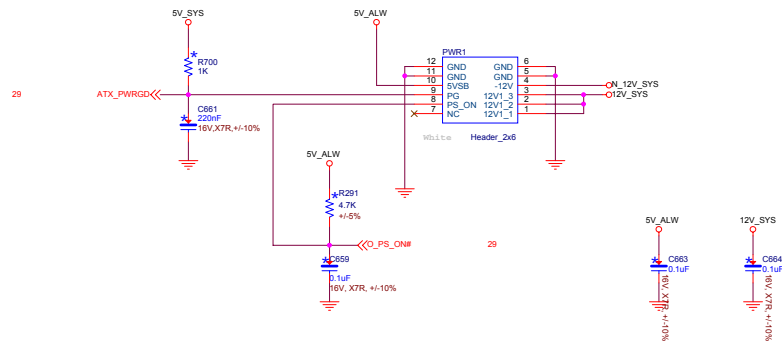
www.aitech1.ru



20120908 For Ri Wakeup 3V\_ALW change to 3D3V\_DUAL

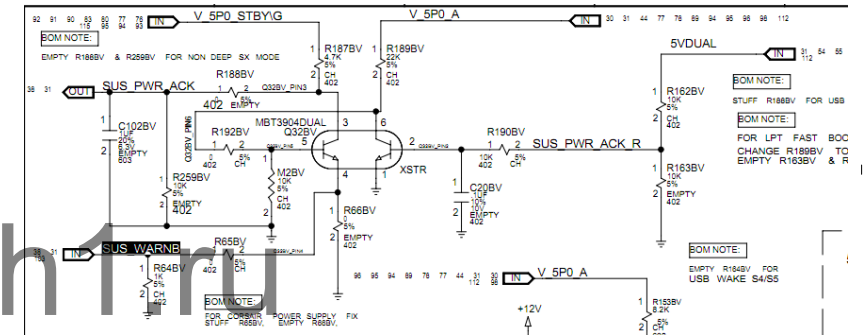
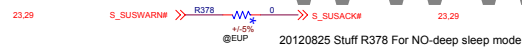


## ATX POWER CONNECTOR



### For Deep Sleep

20120912c delete reserved deep sleep sch

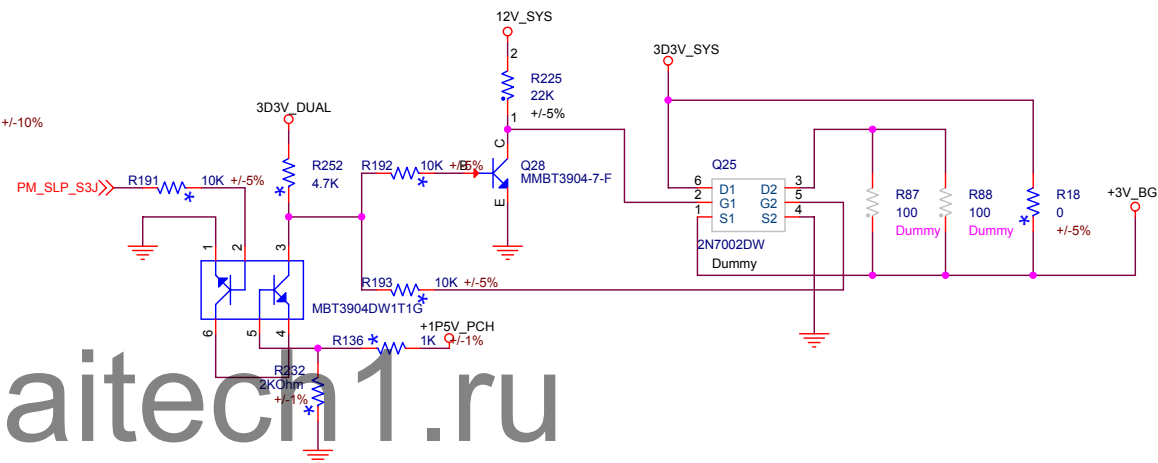
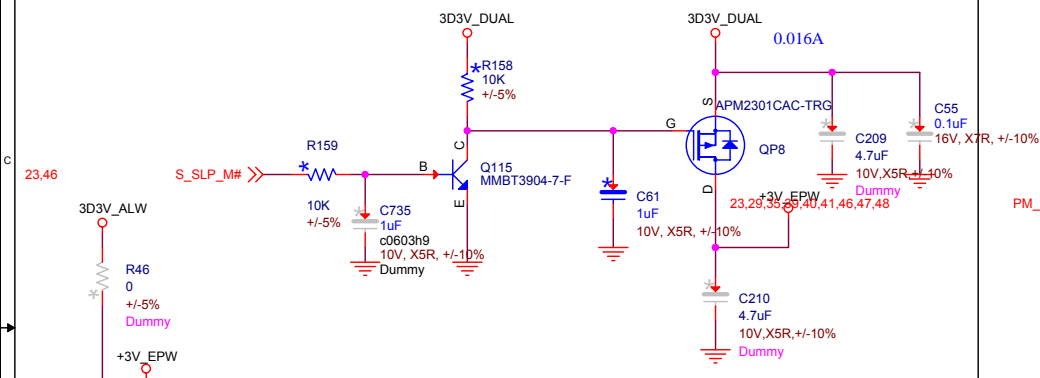


+3V\_EPW

+3V\_BG

20120910

因时序要求,将SLP\_S3&1P5V\_PCH控制线路Reserved

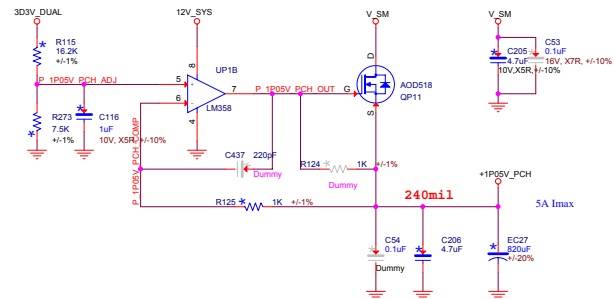


**FOXCONN**

FOXCONN PCEG

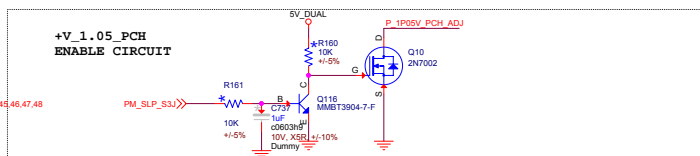
Title		
Power-1: Linear Power-1		
Size	Document Number	Rev
B	SPARTAN	A
Date:	Thursday, March 07, 2013	Sheet 45 of 54

## +1P05\_PCH

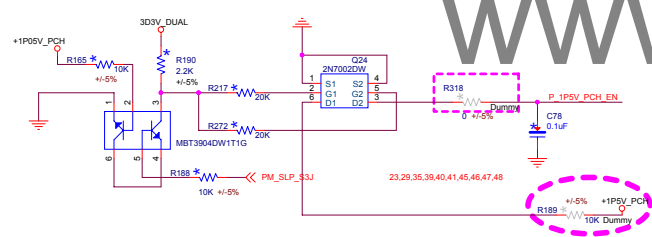


20120910  
因时序要求,1D05V\_PCH比3V\_PG先High且比1D5V\_PCH先High

20121108 EC27 100uF change to 820uF

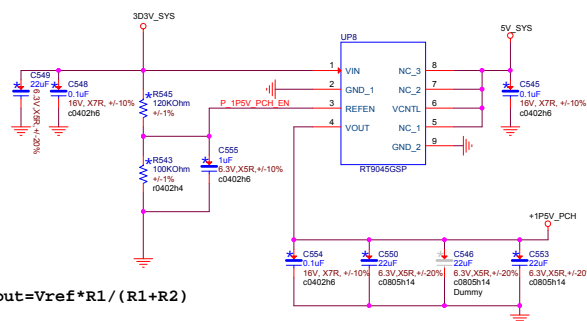


23.29.35.39.40.41.45.46.47.48

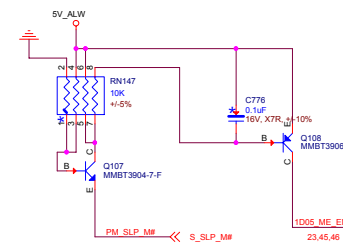


23,29,35,39,40,41,45,46,47,48

— **THE** —

$$V_{out} = V_{ref} * R1 / (R1 + R2)$$


## +V\_1.05\_ME

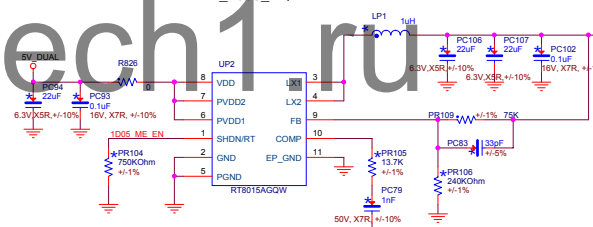


20120829 Change ME Power IC

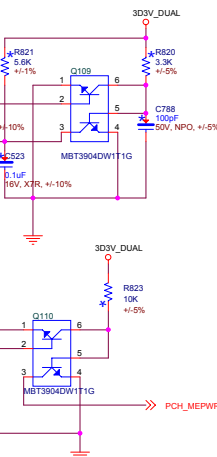
	S5	S0
S_SLP_M#	S_SLP_M#-L Q107手通	S_SLP_M#-H Q107截止
1D05_ME_EN	1D05_ME_EN-H IIP2-Shutdown	1D05_ME_EN-H IIP2-Work

20120922 for Intel ME Request  
ME Power series 0ohm for DSW&EUP

+V\_1.05\_ME/2A

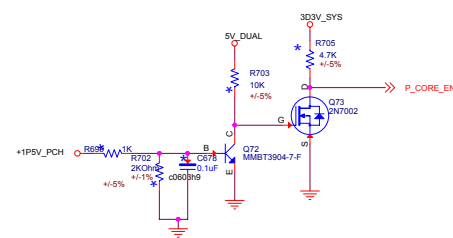


20120911 SHDN/RT Forcing this pin to VDD causes the device to be shut down



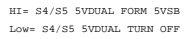
20120830  
Support Intel Small Business Advantage  
Platforms that support M3 power states without the ability to  
communicate with Intel ME via LAN

20120914 For ME Reserved



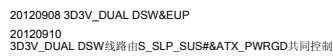
File		Power-2: 1.05V_PCH/ME	
Size	Document Number	<b>SPARTAN</b>	
A2			
Date:	Thursday, March 07, 2013	Sheet	46 of 54

20120830  
5VSB\_CTRL#在开EUP进S5时为High,Eup Disable S0/S3/S4/S5时为Low  
20120911d Add S\_SLP\_SUS control 5V\_DUAL&USB Power

20120825 S\_SLP\_SUS R49 For deep sleep mode

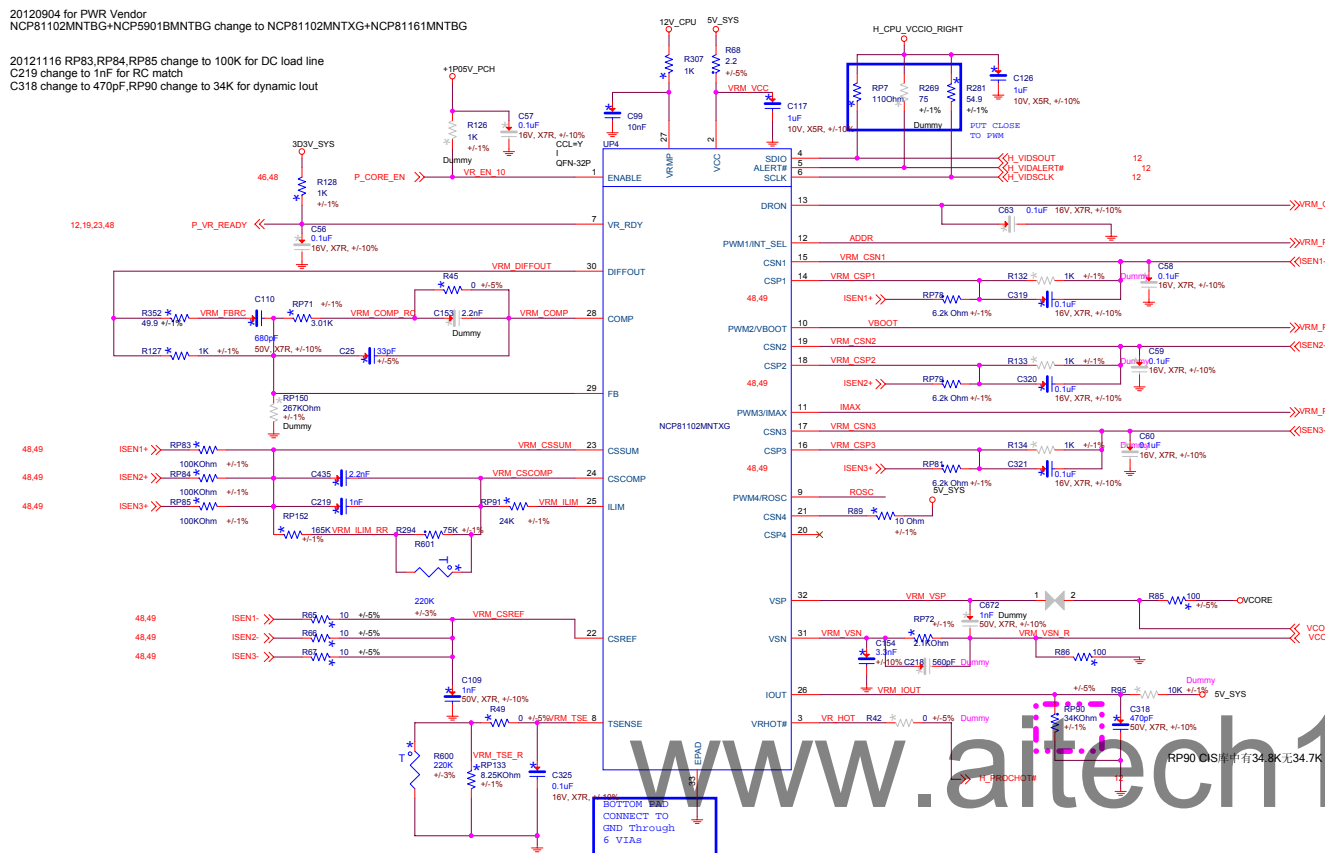
Signal Name	Power Plane	During Reset <sup>1</sup>	Immediately after Reset <sup>1</sup>	S0/S1	S3	S4/S5
SLP_SUS# <sup>17</sup>	DSW	Low	High	High	High	High

Max. output current = 3A



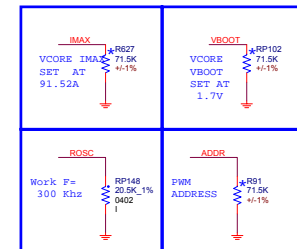
20120904 for PWR Vendor  
NCP81102MNTBG+NCP5901BMNTBG change to NCP81102MNTXG+NCP81161MNTBG

20121116 RP83,RP84,RP85 change to 100K for DC load line  
C219 change to 1nF for RC match  
C318 change to 470pF,RP90 change to 34K for dynamic load



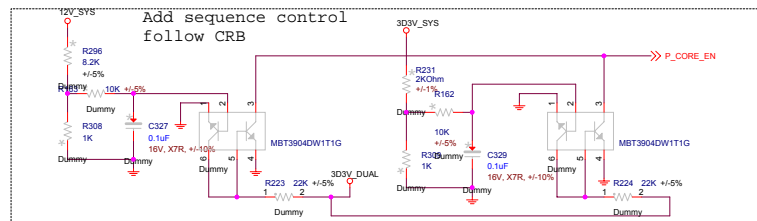
20120921 Due to PDG1.5 change Max current to 90A for 95W CPU.  
LL around 1.54mohm; OCP around 155A  
So R627 change to 71.5K for IMAX set 91~92A,  
RP90 change to 34.7K for load setting  
Change VCC pin resistor R68 to 2.2ohm form 10ohm

$$I_{CC\_MAX} = \frac{R \cdot (0.01 \cdot 256)}{2V}$$
$$R_{OCP} = \frac{2.0V \cdot R_{IMAX}}{R_{CS1} + R_{CS1} \cdot R_{th}} \cdot \frac{1}{10 \cdot \frac{R_{CS1} + R_{th}}{R_{ph}} \cdot (I_{OCP\_SET} \cdot DCR)}$$

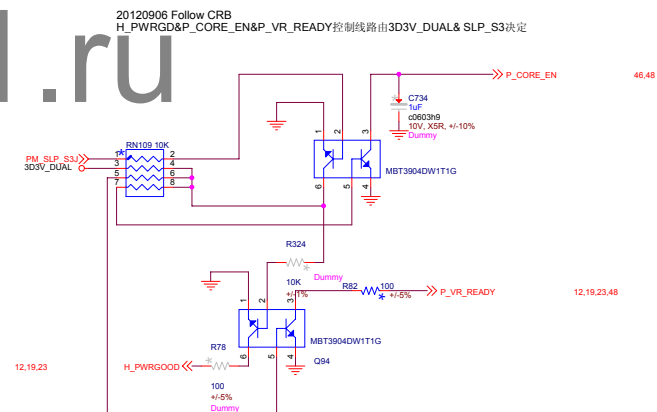


Rosc	Freq.	Rosc	Freq.	Rosc	Freq.	Rosc	Freq.	Rosc	Freq.
10K	250KHz	30.9K	340KHz	61.9K	430KHz	105K	520KHz	165K	610KHz
12K	260KHz	34K	350KHz	64.9K	440KHz	110K	530KHz	174K	620KHz
14K	270KHz	36.5K	360KHz	69.8K	450KHz	115K	540KHz	182K	630KHz
16.2K	280KHz	40.2K	370KHz	73.2K	460KHz	121K	550KHz	191K	640KHz
18.2K	290KHz	43.2K	380KHz	78.7K	470KHz	130K	560KHz	200K	650KHz
20.5K	300KHz	46.4K	390KHz	82.5K	480KHz	137K	570KHz		
23.2K	310KHz	49.9K	400KHz	88.7K	490KHz	143K	580KHz		
25.5K	320KHz	53.6K	410KHz	93.1K	500KHz	150K	590KHz		
28K	330KHz	57.6K	420KHz	100K	510KHz	158K	600KHz		

PWM ADDRESS		BOOT VOLTAGE	
RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	RESISTOR VALUE	BOOT VOLTAGE
10K	0000	30.1K	0V
25K	0010	49.9K	1.65V
45K	0100	39.8K	1.7V
70K	0110	90.9K	1.75V
95K	1000	130K	0V
125K	1010	150K	1.65V
165K	1100	169K	1.7V
		OPEN	1.75V



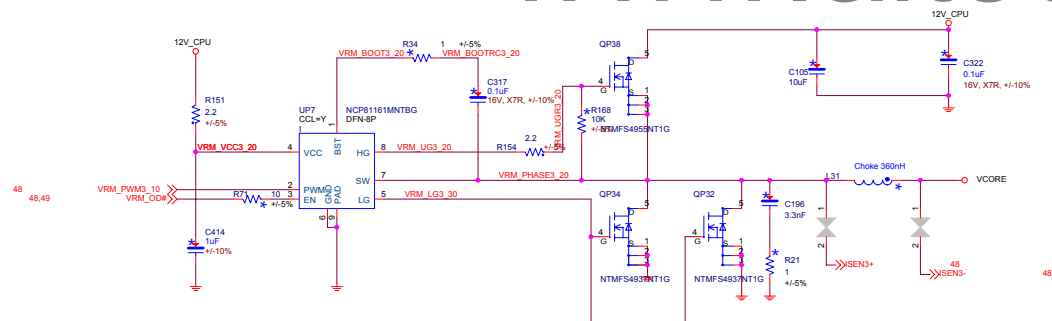
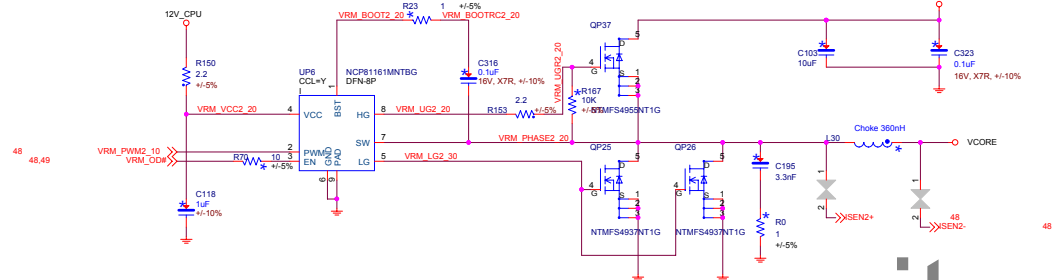
20120906 P\_CORE\_EN by 12V\_SYS&30V\_SYS control line Dummy



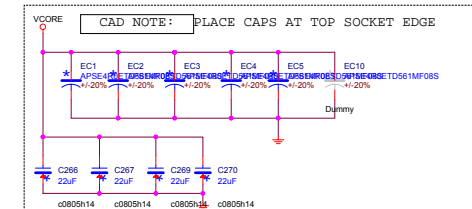
20121110 Stuff Q94&R82 for P\_VR\_READY(SYS\_PWROK) glitch during shutdown



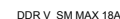
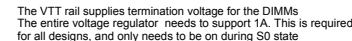
20120911 VCORE Chock L29&L30&L31 change from SMD to DIP



Part Number Description	Rated voltage (VDC)	Rated Capacitance (μF)	tanδ	Leakage Current (μA)	E S R 100-300kHz at 20°C (mΩ)	Rated ripple current 100kHz at105°C (mA r.m.s.)	Dimensions (mm)	
							φD	L
APSC160ELL271MHB5S	16	270	0.10	864	11	5080	8	11.5



Max=40A  
25A in design guide

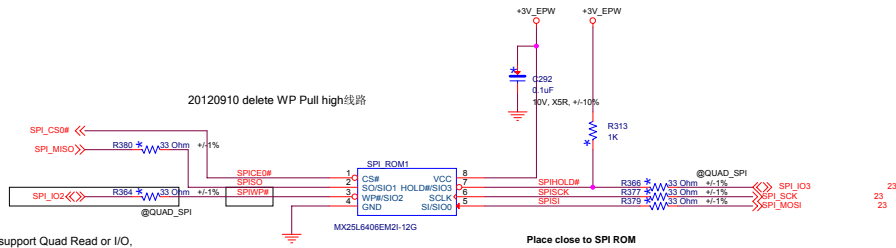


20121010 updata LP14 Footprint&amp; HH P/N



## SPI SOCKET Primary

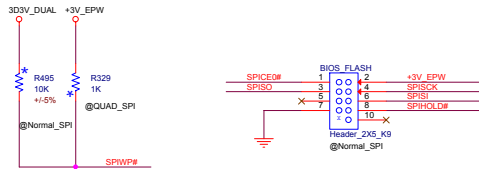
20120910 delete WP Pull high线路



Place close to SPI ROM

20120912 Add SPI Socket  
SPI signal--Serial Input&Serial  
Output&I/O2&I/O3&Clock need series  
resistor, I/O2&I/O3 need pull high

For platform support BIOS WP



Support Quad Read I/O Rom parts. (Beaware of 2nd source  
need to be support Quad I/O read)

## 3. PIN CONFIGURATION SOIC 150 / 208-MIL

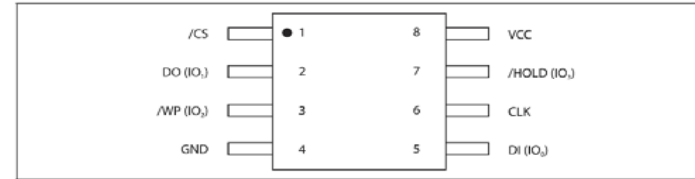


Figure 1a. W25Q16CV Pin Assignments, 8-pin SOIC 150 / 208-mil (Package Code SN & SS)

## PIN DESCRIPTION SOIC 150/208-MIL, PDIP 300-MIL AND WSON 6X5-MM

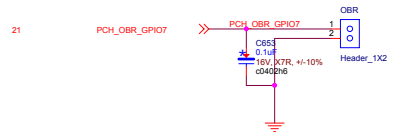
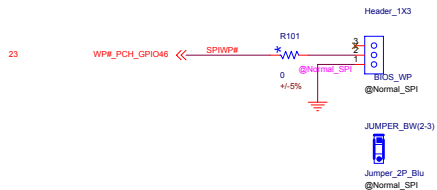
PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)* <sup>1</sup>
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)* <sup>2</sup>
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)* <sup>1</sup>
6	CLK	I	Serial Clock Input
7	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)* <sup>2</sup>
8	VCC		Power Supply

\*1 IO0 and IO1 are used for Standard and Dual SPI instructions

\*2 IO0 – IO3 are used for Quad SPI instructions

20120827 BIOS WP Change from 2Pin to 3Pin

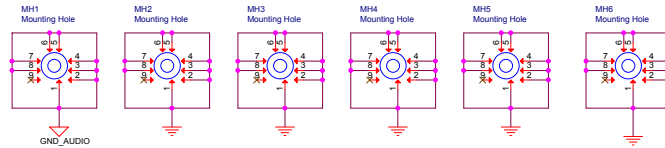
pin 1-2 enable ,pin 2-3 disable,  
default setting is disable



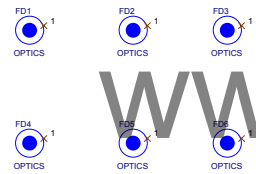
**FOXCONN**  
FOXCONN PCEG

SPI_Socket_ROM			
Rev	Document Number	Rev	
A2		A	
SPARTAN			
Thursday, March 07, 2013			

20120917 For Audio GND



20120824 EMI MLCC Delete (由Layout决定)



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